ECL & INSTRUMENTATION INTEGRATED CIRCUIT HANDBOOK

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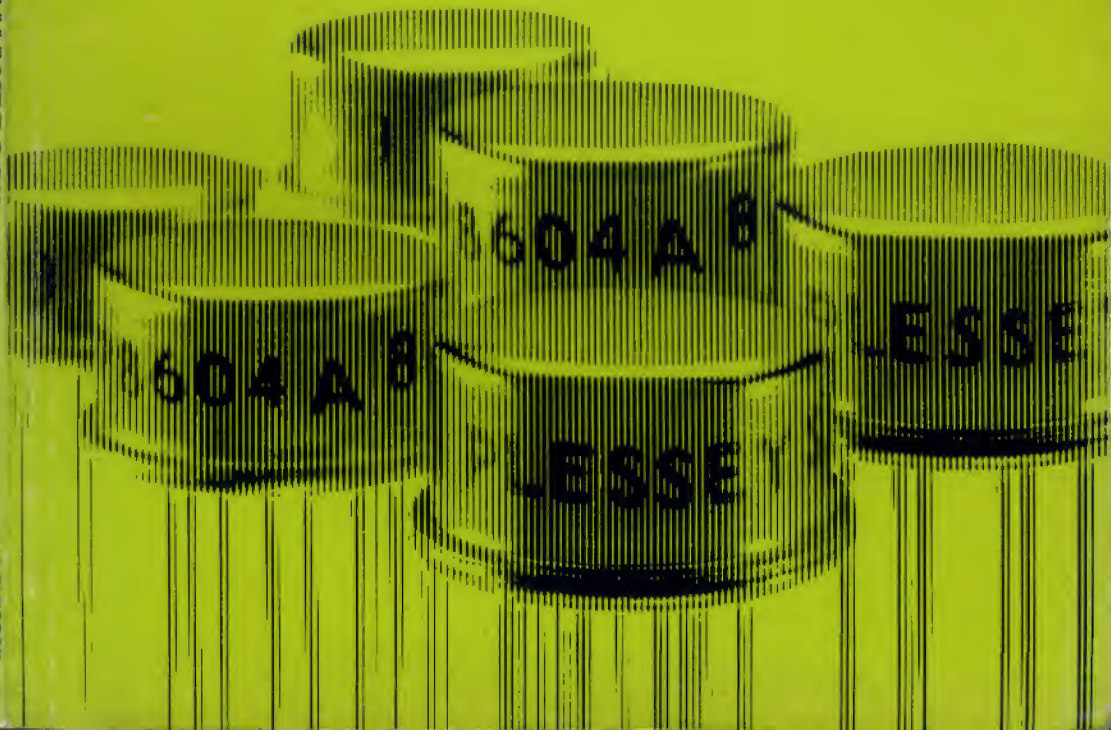
Semiconductors



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Designed and produced by Peter Wigens Consultants

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Contents

Product Index

*The SP16F60, SP16F70, SP9131, SP9685 and SP9687 are pin-compatible higher performance versions of the equivalents shown.

SP8000 series high speed dividers

Essential data for the SP8000 series high speed dividers is given below. Full technical data for these products is published separately in Plessey Semiconductors SP8000 series High Speed Dividers Handbook.

Plessey Semiconductors' SP8000 series leads the world in technical performance. One of the most comprehensive ranges of dividers available, the SP8000 series has been developed and extended to cater for the exacting requirements of the instrumentation and communications markets. The range includes prescalers from divide-by-2 up to divide-by-256, operating from 1Hz to 1.5GHz.

Suffix A Military	-55°C to +125°C
Suffix M Intermediate	-40°C to +85°C
Suffix B Commercial	-30°C to +70°C
	(0°C to +70°C in some cases)

FIXED MODULUS PRESCALERS

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Output		Package		
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	Metal can	Ceramic	Plastic
2	SP8604A	●				300		●			12		●	●		
	SP8604B			●		300		●			12		●	●		
	SP8602A	●				500		●			12		●	●		
	SP8602B			●		500		●			12		●	●		
	SP8607A	●				600		●			14		●	●		
	SP8607B			●		600		●			14		●	●		
	SP8605A	●				1000		●			70		●		●	
	SP8605B				●	1000		●			70		●		●	
	SP8606A	●				1300		●			70		●		●	
	SP8606B				●	1300		●			70		●		●	
4	SP8790A	●				60	●	●			8	●		●		
	SP8790B			●		60	●	●			8	●		●		
	SP8601A	●				150		●			18	●	●	●		
	SP8601B			●		150		●			18	●	●	●		
	SP8600A	●				250		●			16	●	●	●		
	SP8600B			●		250		●			16	●	●	●		
	SP8610A	●				1000		●			70		●		●	
	SP8610B				●	1000		●			70		●		●	
	SP8617M		●			1300			●		80		●		●	
	SP8617B				●	1300			●		80		●		●	
	SP8611A	●				1300		●			70		●		●	
	SP8611B				●	1500		●			70		●		●	
	SP8619M		●			1500			●		80		●		●	
	SP8619B				●	1500			●		80		●		●	
5	SP8620A	●				400		●			55		●		●	
	SP8620B			●		400		●			55		●		●	

FIXED MODULUS PRESCALERS (CONTINUED)

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	Metal can	Ceramic	Plastic
8	SP8794A	●				120	●	●			10	●		●		
	SP8794B			●		120	●	●			10	●		●		
	SP8670A	●				600		●			45		●		●	
	SP8670B			●		600		●			45		●		●	
	SP8735B				●	600		●			70	Ⓑ	●		●	
	SP8675B				●	1000			●		70		●		●	
	SP8678B				●	1500			●		70		●		●	
10	SP8660A	●				150	●	●			10	●		●		
	SP8660B			●		150	●	●			10	●		●		
	SP8660			●		150	●	●			10	●				●
	SP8632B			●		400		●			70		●		●	●
	SP8637B				●	400		●			75	Ⓑ	●		●	
	SP8630A	●				600		●			70		●		●	
	SP8630B			●		600		●			70		●		●	●
	SP8635B				●	600		●			75	Ⓑ	●		●	
	SP8634B				●	700		●			75	Ⓑ	●		●	
	SP8665B				●	1000			●		80		●		●	
	SP8668B				●	1500			●		80		●		●	
16	SP8659A	●				200	●	●			10	●		●		
	SP8659B			●		200	●	●			10	●		●		
	SP8650A	●				600		●			45		●		●	
	SP8650B			●		600		●			45		●		●	
20	SP8657A	●				200	●	●			10	●		●		
	SP8657B			●		200	●	●			10	●		●		
	SP8658			●		200	●	●			20	●				●
32	SP8655A	●				200	●	●			10	●		●		
	SP8655B			●		200	●	●			10	●		●		
64	SP8755A	●				1200	●				45	●			●	
	SP8755B			●		1200	●				45	●			●	
	SP8757			●		1200		●			45		●			●
100	SP8628			●		150	●	●			33	●				●
	SP8629			●		150	●	●			33	●				●
256	SP8775			●		1200	●				70	●				●

Ⓑ = Binary outputs

VARIABLE-MODULUS PRESCALERS

The two-modulus dividers will divide by either of two ratios according to the state of a control input compatible with ECL, TTL or CMOS as shown. Further division ratios can be obtained by means of extra prescalers. For example, by using the SP8790 (÷4) or SP8794 (÷8) — which are specially designed for extending the ratio of two-modulus dividers and have TTL compatible control inputs — it is possible to extend a ÷10/11 to 40/41 or 80/81 respectively.

Use of variable modulus dividers to obtain fixed division ratios.

Any of the variable modulus dividers can be simply connected to divide permanently by either modulus. For example the SP8691 ÷8/9 can become a fixed ÷8 or ÷9 by hardwiring the appropriate programming pins. This technique (described in the datasheets) extends the range of fixed prescalers to include division ratios of 3, 6, 7, 9, 11, 22, 40, 41, 80 and 81.

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Control input		Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	TTL	ECL	Metal can	Ceramic	Plastic
3/4	SP8720A	●				300		●			40		●		●		●	
	SP8720B			●		300		●			40		●		●		●	
5/6	SP8740A	●				300		●			45		●		●		●	
	SP8740B			●		300		●			45		●		●		●	
6/7	SP8741A	●				300		●			45		●		●		●	
	SP8741B			●		300		●			45		●		●		●	
8/9	SP8691A	●				200	●	●			14		●	●	●		●	
	SP8691B			●		200	●	●			14		●	●	●		●	
	SP8743A	●				500		●			45		●		●		●	
	SP8743B			●		500		●			45		●		●		●	
10/11	SP8690A	●				200	●	●			14		●	●	●		●	
	SP8690B			●		200	●	●			14		●	●	●		●	
	SP8647A	●				250	●	●			50		●	●	●		●	
	SP8647B			●		250	●	●			50		●	●	●		●	●
	SP8643A	●				350	●	●			50		●		●		●	
	SP8685A	●				500		●			45		●		●		●	
	SP8685B			●		500		●			45		●		●		●	
	SP8680A	●				600	●	●			90		●	●	●		●	
	SP8680B				●	600	●	●			90		●	●	●		●	
20/22	SP8785A	●				1000		●			85		●		●		●	
	SP8785B				●	1000		●			85		●		●		●	
	SP8786A	●				1300		●			85		●		●		●	
	SP8786B				●	1300		●			85		●		●		●	

VARIABLE-MODULUS PRESCALERS (CONTINUED)

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Control input		Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	TTL	ECL	Metal can	Ceramic	Plastic
40/41	SP8793A	●				200		●			4	●		●			●	
	SP8793			●		225		●			4	●		●				●
80/81	SP8792A	●				200		●			4	●		●			●	
	SP8792			●		225		●			4	●		●				●

Quality data

Plessey Semiconductors have an active **BS9300** and **BS9400** qualification approval programme on a number of products.
Additionally, Plessey Semiconductors are keen to co-operate in pursuing **BS9000** approval on any of the products which it manufactures.
For further information contact the Military Marketing Group at Swindon.

Plessey Semiconductors QA offers:

a) Factory Approval to

BS9300 for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)

BS9400 for integrated circuits of Assessed Quality (BSI Certificate 1053/M)

CECC 50000 Inspection Organisation to document level 1 (BS9300) M0020/CECC refers

DEF STAN 05—21 QC System requirements for Industry (Equivalent to AQAP—1) Certificate 65752/1/01 refers

b) Additional Release Conditions to

6/49 Defence Quality Assurance Board Certificate (DQAB 38020)

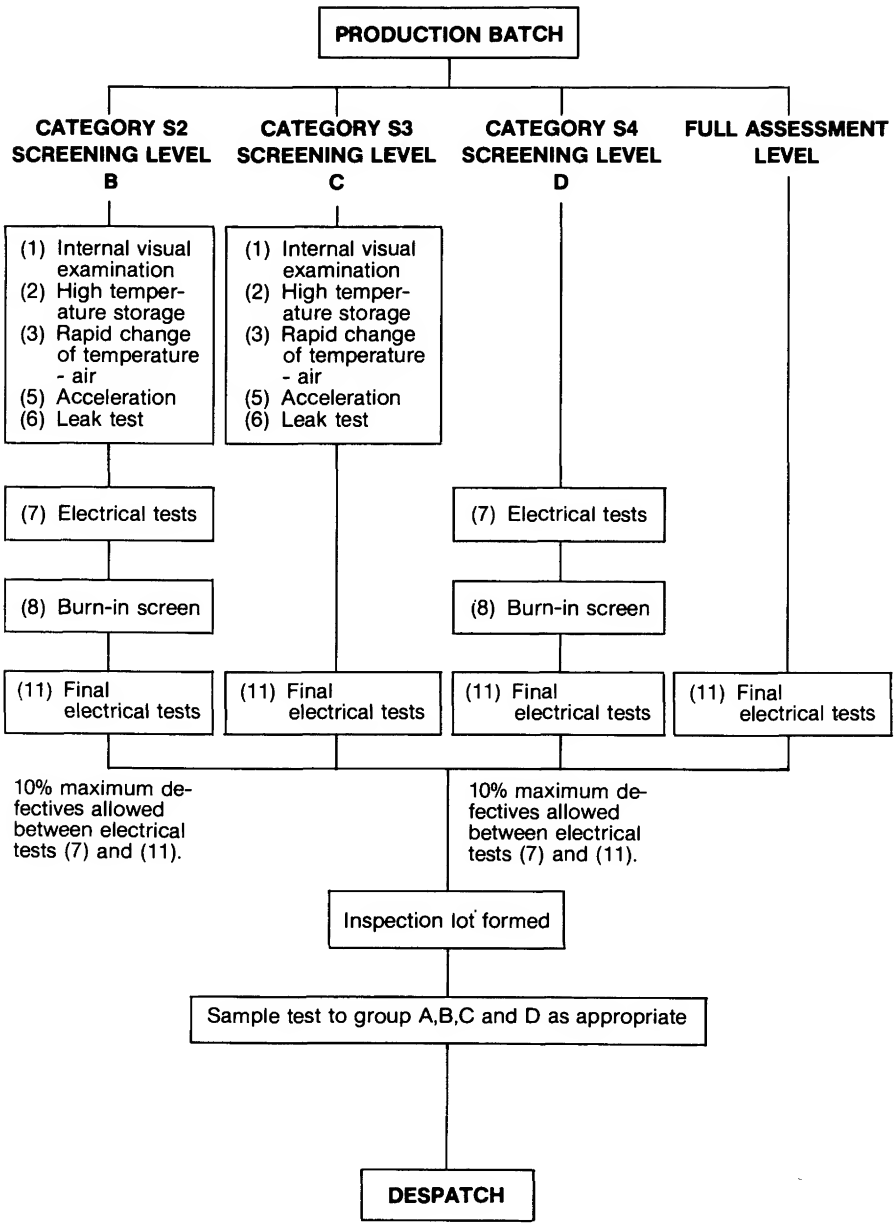
MOD (N) Navy Department Inspection Authority

or

Private Sales Plessey's own Certificate of Conformance

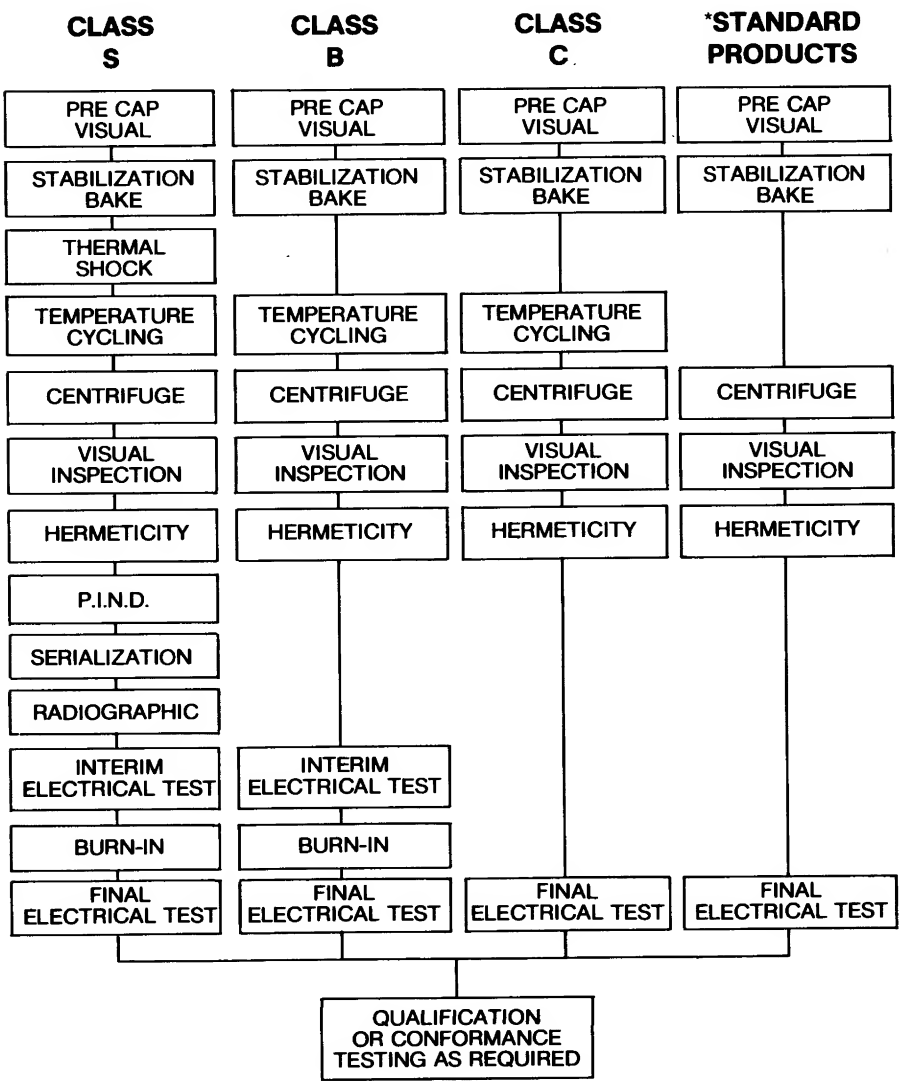
Devices are also manufactured, tested and supplied to **MIL-STD-833**, the US Military Standard; Test Methods and Procedures for Microcircuits, and **MIL-M-38510**, US Military Specification, Micro-electronics; General Specifications for.

Screening to BS9400



Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom design

Semi-custom design techniques give users the advantages of integrated circuits dedicated to their applications without incurring the costs associated with full custom design. The techniques are particularly attractive to users with a low-to-moderate annual production potential of 1000 to 100,000 pieces, although these limits are flexible and may depend on the individual circuit. The economics of 'when to choose semi-custom' are illustrated in Fig.1.

Plessey Semiconductors offer semi-custom facilities in N-Channel MOS, CMOS and Bipolar technologies, using the techniques of Microcell, Gate Arrays and Analogue Arrays, the essential characteristics of which are detailed in Table 1.

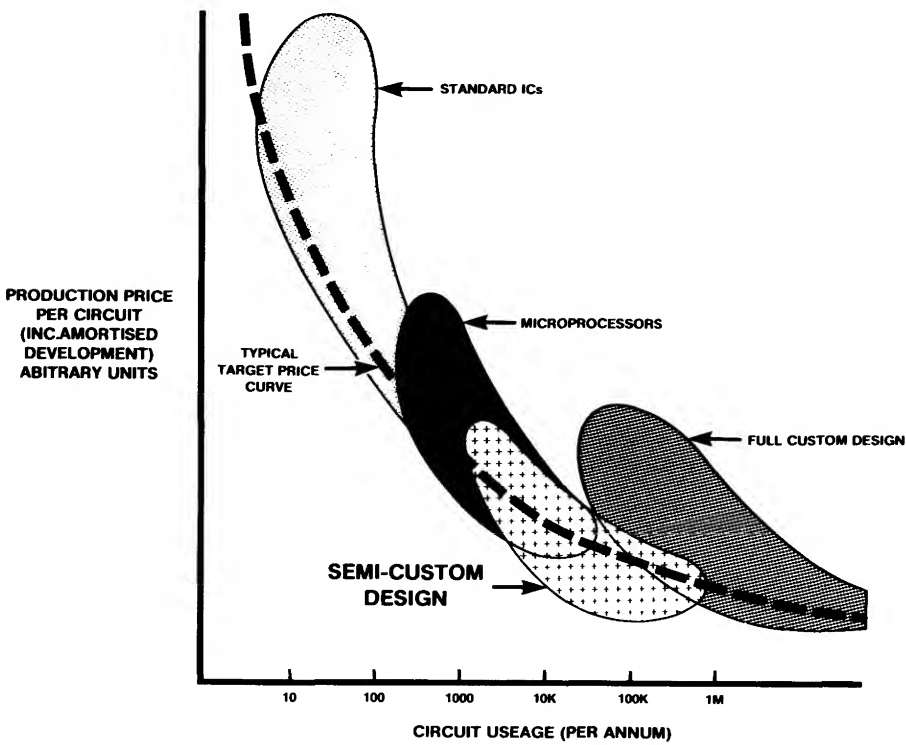


Fig 1 Areas of application of different categories of integrated circuits

MICROCELL

Microcell is a combination of standard cells with a formalised gate and interconnection procedure. It uses a computer library of gates and other cells which the designer calls up as required, leaving as much or as little space for interconnection as the design necessitates. Each circuit is exactly the right size for its

function, and layout for the interconnection pattern is both straightforward and fast because of the error-correcting digitising technique employed.

The main features of Microcell can be summarised as follows: • From logic diagram to first samples in less than four months • Very high design integrity • A circuit can be produced by any competent logic designer • Minimal extra engineering effort is required • Clock rates of up to at least 2MHz are achievable • Advances in semiconductor technology and circuit design ideas can easily be absorbed into Microcell.

GATE ARRAYS

In the Gate Array, logic elements are pre-positioned and the customer's task is to design the interconnection of those elements (within the space allocated) to achieve the required functions. The cells are not necessarily committed to logic functions, but may in some cases be connected to form simple linear functions. Layout aids and software routines are normally used extensively to assist in the design, verification and testing of these structured devices.

Plessey Semiconductors offer Gate Array techniques in CMOS and ECL. CMOS Gate Arrays offer the following features: • High Speed ISO-CMOS Silicon Gate technology, giving a typical propagation delay of 6ns for a 2-input NAND gate (at 5V and 25°C) • Short turn round time • Inputs and outputs TTL and CMOS compatible and provided with static protection • On-chip power on reset option available • Available to commercial, industrial and military standards.

ECL Gate Arrays - also possessing the advantages of low development charge, increased reliability and fast delivery of samples - would be chosen mainly for the very high speed operating capability.

ANALOGUE ARRAYS

Plessey Semiconductors' Analogue Array brings Semi-Custom techniques to the designer of linear and other analogue circuits, for applications such as signal processing, amplification, waveform generation and function generation.

Manufactured on Bipolar Process I the analogue array features: • 159 NPN transistors (4 high current) • 58 PNP transistors • 385 resistors • 20V breakdown voltage • Functional compatibility with Exar and Interdesign • Single layer customisation on a grid system • Device library and simulation facilities.

Comprehensive technical literature on all Plessey Semiconductors' Semi-Custom Facilities is available on request.

SEMI-CUSTOM OPTION	TECHNOLOGY	SPEED	POWER CONSUMPTION	SCALE OF INTEGRATION	TYP. LEAD TIME TO 1ST SAMPLES
NMOS Microcell	NMOS Metal Gate	2MHz	300mW/1000 gates	500-2500 gates	16 weeks
Low Power NMOS Microcell	NMOS Metal Gate	0.5MHz	50mW/1000 gates	500-2000 gates	16 weeks
CMOS Microcell	ISO-CMOS	10MHz	0-150mW/1000 gates*	500-2000 gates	16 weeks
CMOS Gate Array	ISO-CMOS	8MHz	0-150mW/1000 gates*	560,960,1440 and 2014 gates	13 weeks
ECL Gate Array	Bipolar Process III	200MHz	75 gates: 900mW max 300 gates: 3.5W max	75 to 600 gates	14 weeks
Bipolar Analogue Array	Bipolar Process I	f_T = 500MHz	100mW to 1W**	217 transistors	16 weeks

* Depending on speed
** Depending on application

Table 1

Technical Data

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SP705B

CRYSTAL CONTROLLED INTEGRATED CIRCUIT OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: $f/2$, $f/4$, $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications

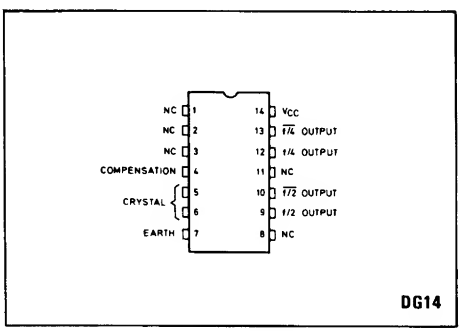

Fig.1 Pin connections

FEATURES

- Operating Frequency up to 10 MHz
- $f/2$ and $f/4$ outputs
- 4 TTL Level outputs
- Operates from +5V TTL Supply

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
High state output voltage	V_{OH}	2.6		V	V_{CC} = 4.75V I_{OH} = 0.2 mA
Low state output voltage	V_{OL}		0.4	V	V_{CC} = 5.25V I_{OL} = 8 mA
Supply current	I_{CC}		35	mA	V_{CC} = 5V
Output rise time (10% to 90%)	t_R		20	ns	V_{CC} = 5V
Output fall time (90% to 10%)	t_F		20	ns	V_{CC} = 5V
Operating frequency (f)			10	MHz	
Operating temp range		0	70	°C	

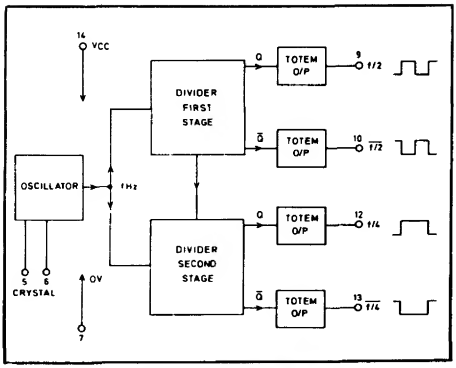

Fig. 2 SP705B block diagram

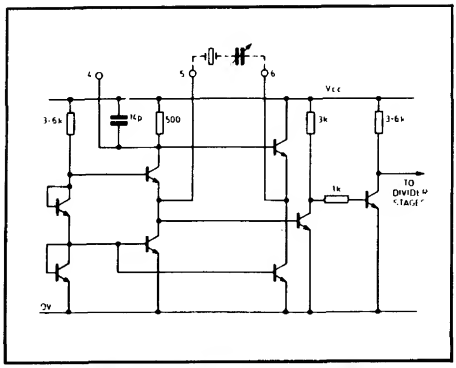

Fig. 3 Circuit diagram of SP705B oscillator

CIRCUIT DESCRIPTION

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with a 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig. 3.

The circuit is designed to provide low crystal drive levels – typically, less than 0.15mW at 5MHz. This is well within crystal manufacturers' limit of 0.5mW.

The compensation point, pin 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

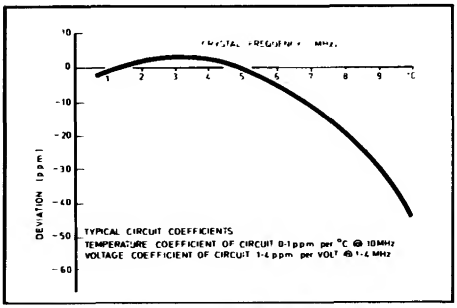

Fig. 4 Deviation from nominal crystal frequency

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SP761B 12V POWER INTERFACE CIRCUIT
SP762B 5V POWER INTERFACE CIRCUIT

The SP761B and SP762B are bipolar integrated circuits, each incorporating five current amplifiers for interfacing between MOS/TTL devices and loads requiring high drive currents. The SP761B is designed to operate from a +12V supply rail and the SP762B from +5V.

Both types are provided with a strobe input which drives two of the amplifiers so that their outputs may be connected in parallel for higher output current capability.

The circuits operate over a temperature range of 0°C to +70°C and are mounted in 14-lead ceramic DIL package.

Although primarily designed to drive printing solenoids in calculators, these circuits can be used in a variety of applications requiring high drive currents.

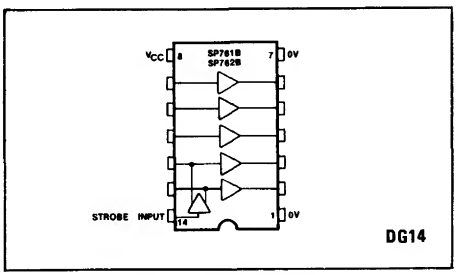


Fig. 1 Pin connections (top)

FEATURES

- Input – MOS/TTL Capability
- Output – 200 mA Capability
- Five Channels per Package
- Open Collector Output

APPLICATIONS

- Driving Solenoids
- Driving Relays
- Driving LEDs
- Driving Filament Lamps
- Driving Cores
- TTL-to-MOS Translator

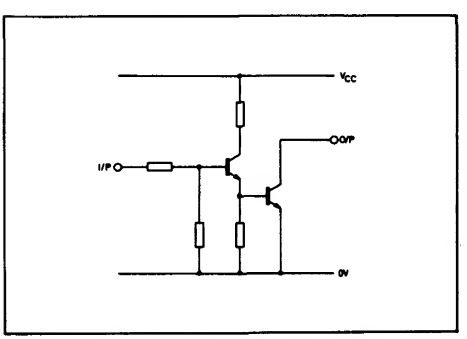


Fig. 2 Functional diagram (one driver)

ABSOLUTE MAXIMUM RATINGS

Output collector voltage	26V
Supply voltage, SP761B	+15V
Supply voltage ,SP762B	+7V
Storage temp.	−55°C to +125°C
Chip operating temp.	+125°C
Ambient operating temp.	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristic	Type	Value (note 1)			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC}	SP761B	11	12	13	V	See note 2
	SP762B	4.5	5	5.5	V	See note 2
Quiescent supply current	SP761B		8		mA	All inputs low
	SP762B		10		mA	All inputs low
On state supply current, per element	Both		12		mA	I_{IH} = 1mA
Input current I_{IH}	SP761B	1		4	mA	I_{out} = 150mA
Input voltage V_{IH}	SP761B		4		V	I_{IH} = 1mA
Input current I_{IL}	SP761B			50	μA	
Input voltage V_{IH}	SP762B	2.7		5.5	V	I_{out} = 200mA
Input current I_{IH}	SP762B		1		mA	V_{IH} = 2.7V
Input voltage V_{IL}	SP762B			1	V	
Output current I_{out}	SP761B			150	mA	I_{IH} = 1mA
	SP762B			200	mA	V_{IH} = 2.7V
Output voltage V_{OL}	SP761B		1.0	1.2	V	I_{out} = 150mA
	SP762B		1.3	1.6	V	I_{out} = 200mA
Output voltage V_{OH}	Both			26	V	
Output breakdown voltage	Both	26			V	See note 3
Duty cycle	SP761B			40	%	All outputs at I_{out} max.
	SP762B			33	%	
On time				2	s	

NOTES

1. Both 0V supply pins 1 and 7 must be connected at all times.
2. Min. and max. limits apply to the temperature range 0°C to +70°C. All typical values are quoted for V_{CC} = Typical and T_{amb} = +25°C.
3. External clamping diodes must be used when driving inductive loads.

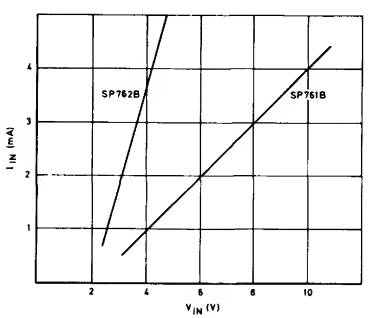


Fig. 3 Input characteristic (including strobe) T_{amb} = +25°C

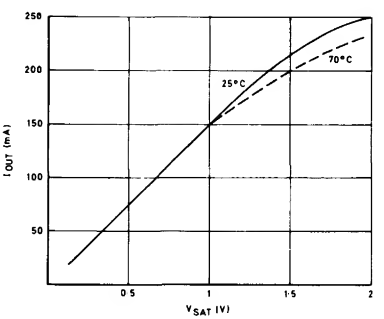


Fig. 4 Output characteristic

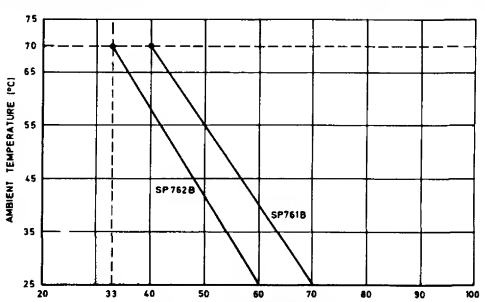


Fig. 5 Operating characteristics

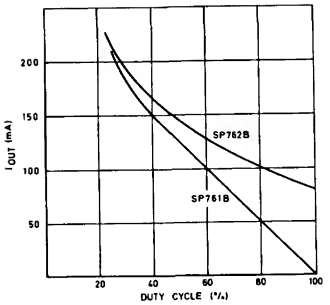


Fig. 6 Operating characteristics at +70°C

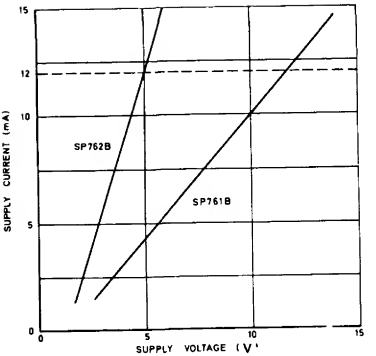


Fig. 7 On state supply current drain per element

OPERATING NOTES

Interfacing

The SP761B is designed to interface directly with MOS devices, accepting free drain input currents in the range 1 mA to 4 mA. Current limiting input resistors are incorporated on-chip to reduce power dissipation in the MOS circuit. The resistor is approximately 2 kΩ, giving an input voltage of 4V at 1 mA.

Fig. 8 shows (i) a direct interface to MOS and (ii) an interface using an external resistor to further limit input current when driven from a high voltage source.

The SP762B will interface directly with standard TTL over the temperature range 0°C to +70°C, a TTL logic '1' making current available at the SP762B output. Although TTL is not specified to source more than 400 μA at logic '1' level, the majority of gates will in fact supply approximately 5 mA and still maintain a logic '1' level in excess of 2.7V. Since the input resistors of the SP762B are approximately 600Ω, then one TTL output is capable of driving up to 5 SP762B inputs. When driving only one input of an SP762B, the input current will limit at approximately 2 mA at 3.4V. Open-collector TTL gates can also be used to drive the SP762B, provided that each TTL output has an external load resistor, the value of which will depend on the fanout required.

The characteristics of the strobe input are the same as for the individual inputs and therefore the above comments also apply to this input.

Unused Inputs

When using the strobe input, inputs 1 and 2 must be left floating. However, inputs 1 and 2 can be used completely independently in the same way as the other inputs. Any other unused inputs can either be left floating or tied to the negative supply rail.

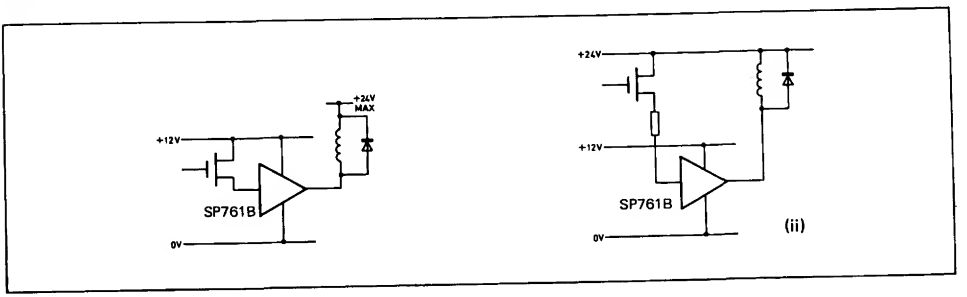
Output Capability

The output capability of each channel is 150 mA for the SP761B and 200 mA for the SP762B. With all five drivers operating at these current levels, a duty cycle of 40% for the SP761B and 33% for the SP762B will allow operation over the temperature range 0°C to +70°C.

If the device is to be operated at a lower ambient temperature, or at a lower output current, then the duty cycle may be increased as shown in Fig. 6 and 7. Likewise, if some of the outputs are unused the duty cycle of the remaining outputs may be proportionally increased provided that the drivers are used symmetrically within the package.

The package has a thermal time constant such that the chip temperature will rise above the permitted maximum of +125°C if all the drivers are allowed to remain on at maximum output current for more than 2 seconds.

The drivers will operate at up to 1 MHz but at such frequencies the input mark/space ratio will have to be modified because the effective output duty cycle is higher than that at the inputs due to stored charge in the output transistors.



PLESSEY
Semiconductors

SP1648

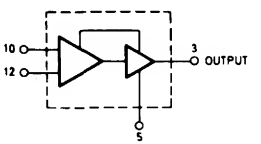
VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8



Input Capacitance = 6pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ.
Power Dissipation = 150mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 Mhz typ

DG14

Fig. 1 Block diagram of SP1648

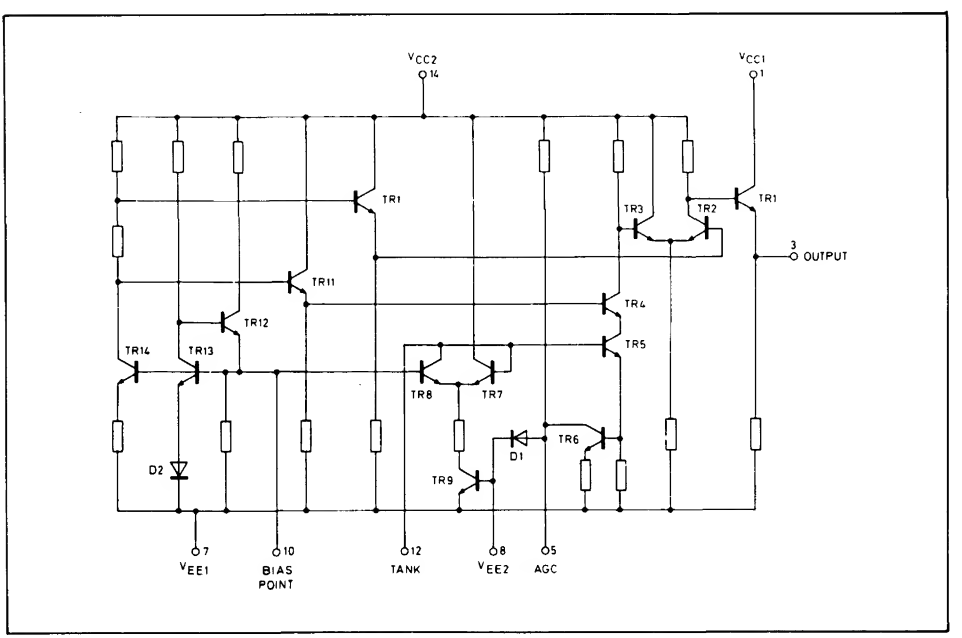


Fig. 2 Circuit diagram of SP1648

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+85°C	+1.680	+1.180	5.0	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	60	—	—	mAdc	—	—	1, 14	—	7, 8
Logic "1" Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1, 14	—	7, 8
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 4	—	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 4	—	1, 14	3	7, 8
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 4	—	1, 14	3	7, 8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

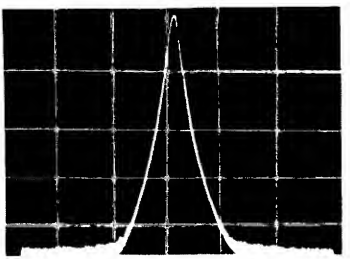
ELECTRICAL CHARACTERISTICS

Supply Voltage = –5.2 volts

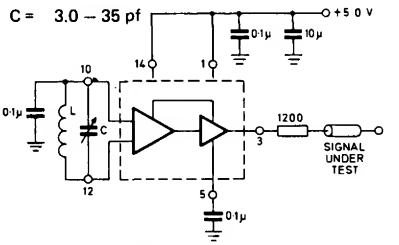
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.240	-3.790	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.520	-4.020	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_{E-C}	8	—	—	—	61	—	—	mAdc	—	—	7, 8	—	1, 14
Logic "1" Output Voltage	V_{OH}	3	1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7, 8	—	1, 14
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 4	—	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 4	—	7, 8	3	1, 14
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 4	—	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

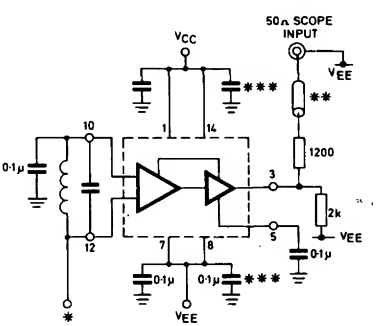


B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10db/div



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Fig. 3 Spectral purity of signal at output



* Use high impedance probe (>1.0 Megohm must be used).

* * The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

* * * Bypass only that supply opposite ground.

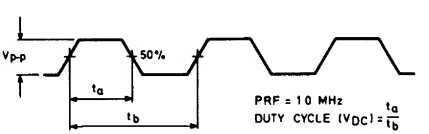


Fig. 4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 thru TR14 provide this bias drive for the oscillator and output buffer. Figure 3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

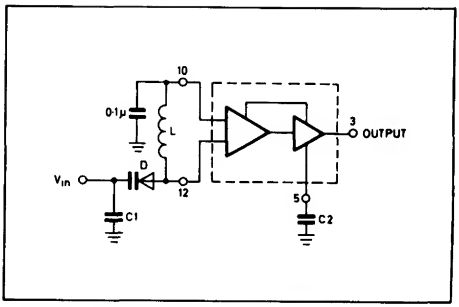


Fig. 5 The SP1648 operating in the voltage-controlled mode

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 6.

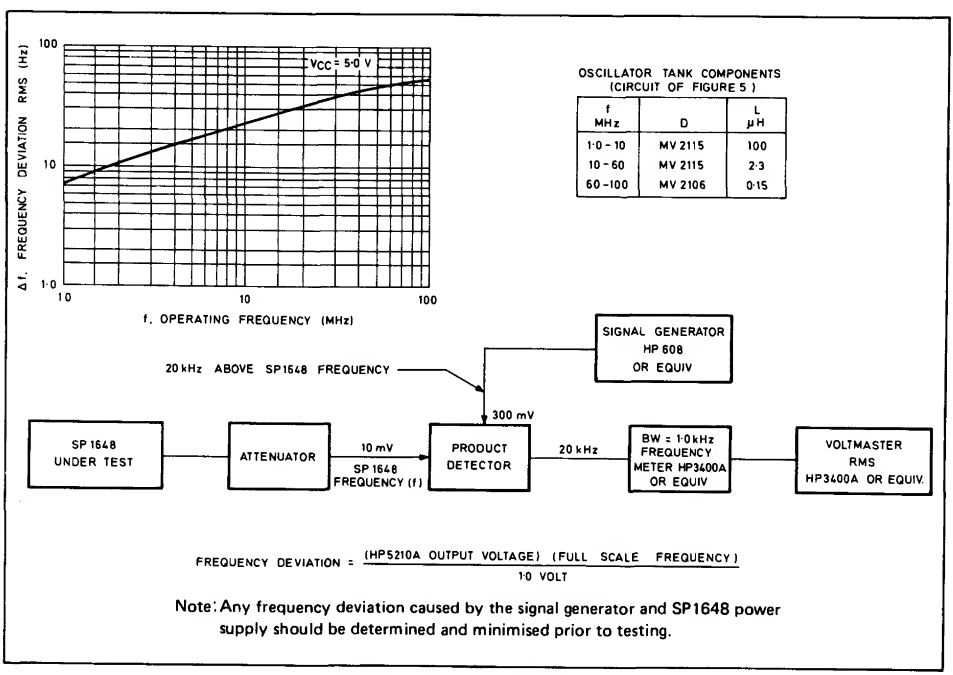
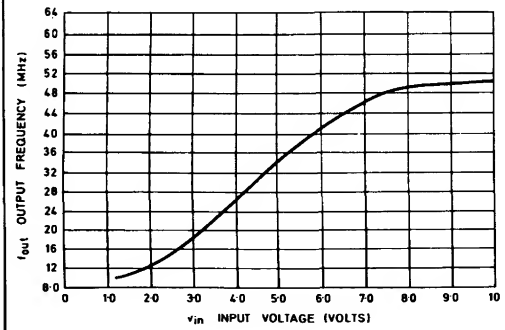
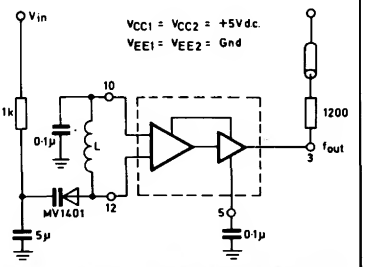


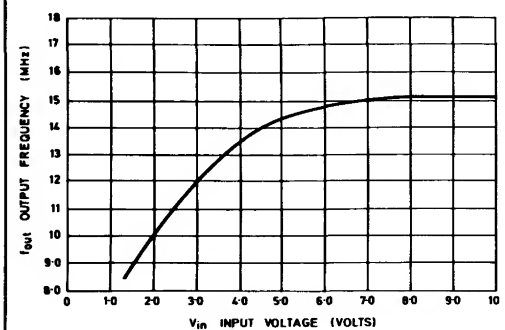
Fig. 6 Frequency deviation test circuit

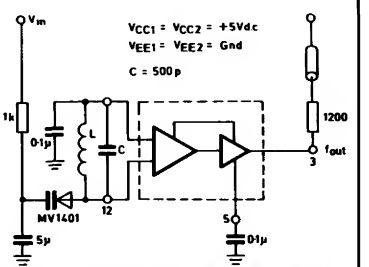




* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

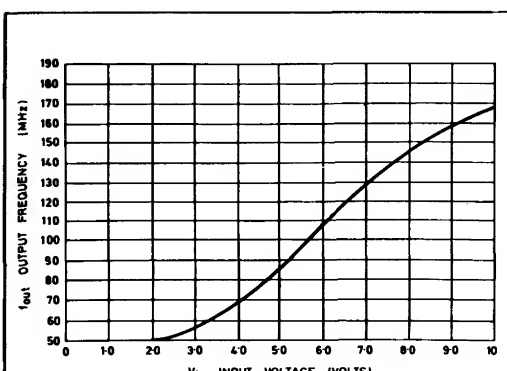
Fig. 7

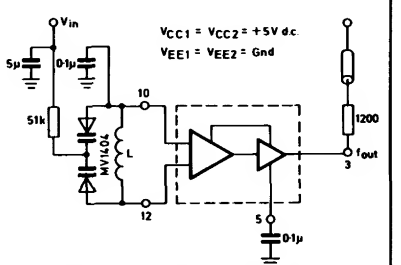




* The 1200 ohm resistor and the scope termination impedance consitute a 25:1 attenuator probe.

Fig. 8





* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Fig. 9

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 7, 8, and 9. Figures 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of of the oscillator, 6pF typical). Figure 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\,(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Figure 3).

Capacitors (C1 and C2 of Figure 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, −5.2 volts if a negative supply is used).

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a −5.2 volt supply is used).

PLESSEY
Semiconductors

SP1650 (HIGH Z)
SP1651 (LOW Z)
DUAL A/D COMPARATOR

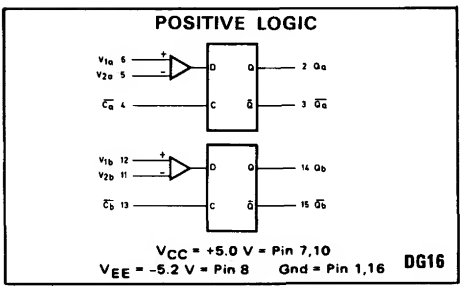


Fig. 1 Logic diagram

FEATURES

- P_D =330mW typ/pkg (No load)
- t_{pd} =3.5ns typ. (SP1650)
  =3.0ns typ. (SP1651)
- Input Slew Rate=350 V/μs (SP1650)
  =500 V/μs (SP1651)
- Differential Input Voltage:
  −5.0V to +5.0V (−30°C to +85°C)
- Common Mode Range:
  −3.0V to +2.5V (−30°C to +85°C) (SP1650)
  −2.5V to +3.0V (−30°C to +85°C) (SP1651)
- Resolution: ≤20mV (−30°C to +85°C)
- Drives 50Ω lines

The SP1650 and the SP1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The SP1650 provides high impedance Darlington inputs, while the SP1651 is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C_a}$ and $\overline{C_b}$) operate from ECL III or ECL 10,000 digital levels. When $\overline{C_a}$ is at a logic high level, Q_a will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q_a}$ is the logic complement of Q_a. When the clock input goes to a low logic level, the outputs are latched in their present state.

Assessment of the performance differences between the SP1650 and the SP1651 may be based upon the relative behaviour shown in Figs. 5 and 8.

TRUTH TABLE

$\overline{C}$	V_1, V_2	Q_{n+1}	$\overline{Q}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	Q_n	$\overline{Q}_n$

ϕ = Don't Care

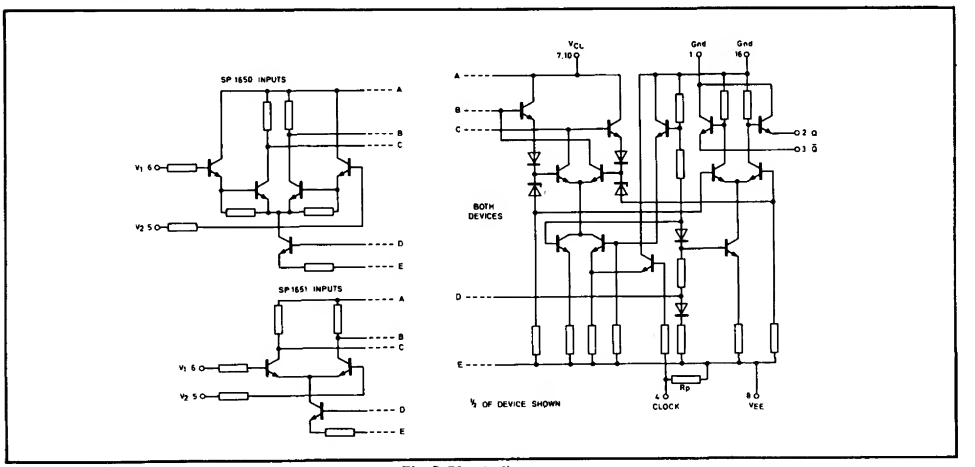


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

● Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits (1) -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10				25*		-	mAdc		4,13			6,12	-	-	-	-	-	7,10	8	1,5,11,16
Negative	I_E	8				55*			mAdc	4,13			-	6,12		-	-	-	-	7,10	8	1,5,11,16
Input Current	I_{in}																					
SP1650		6				10			µAdc	4	13			12	-	6	-	-	-	7,10	8	1,5,11,16
SP1651		6			-	40			µAdc	4	13			12		6	-	-	-	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
SP1650		6				7			µAdc	4	13			12	-	-	-	6	-	7,10	8	1,5,11,16
SP1651		6				10			µAdc	4	13			12	-	-	-	6	-	7,10	8	1,5,11,16
Input Clock Current	I_{inH}	4		-		350		-	µAdc	4	13			6,12		-	-	-	-	7,10	8	1,5,11,16
	I_{inL}	4		-	0.5	-	-	-	µAdc	-	13		-	6,12	-	-	-	-	-	7,10	4.8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13				6,12				-	-	7,10	8	1,5,11,16
		2													5,11	-	-	-	-			1,6,12,16
		2												-		6,12	5,11	-	-			1,16
		2																5,11	6,12			1,16
		3													6,12	-		-	-			1,5,11,16
		3												5,11		-	-	-	-			1,6,12,16
		3												-		5,11	6,12	-	-			1,16
		3														-	-	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13					6,12	-	-	-	-	7,10	8	1,5,11,16
		2												5,11		-	-	-	-			1,6,12,16
		2														5,11	6,12	-	-			1,16
		2														-	-	6,12	5,11			1,16
		3												6,12		-	-	-	-			1,5,11,16
		3													5,11	-	-	-	-			1,6,12,16
		3														6,12	5,11	-	-			1,16
		3														-	-	5,11	6,12			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	1																				
		2	-1.065	-	-0.980	-	-0.910	-	Vdc		13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
		2		-		-		-				-	4	-	6	-	-	-	-			
		3		-		-		-				4	-	-	6	-	-	-	-			
		4		-		-		-				-	4	6	-	-	-	-	-			
Logic "0" Threshold Voltage ②	V_{OLA}	1																				
		2	-	-1.630	-	-1.600		-1.555	Vdc		13	4	-	6		-	-	-	-	7,10	8	1,5,16
		3		-		-						-	4		6	-	-	-	-			
		2	-	-	-	-	-	-				4	-	-	6	-	-	-	-			
		4	-	-	-	-		-				-	4	6	-	-	-	-	-			

NOTES: ① All data is for ½ SP1650 or SP1651 except data marked (*) which refers to the entire package
② These tests done in order indicated. See Figure 6
③ Maximum Power Supply Voltages (beyond which device life may be impaired):
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
SP1650	+3.000	+2.980	-2.500	-2.480
SP1651	+2.500	+2.480	-3.000	-2.980

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

See Figure 4

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times																				
Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2								–	–	5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3	↓	↓	↓	↓	↓	↓	↓	–	–	5	↓	↓	↓	↓	–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2	↓	↓	↓	↓	↓	↓	↓	6	–	–	–	↓	↓	↓	5	–	–	↓
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

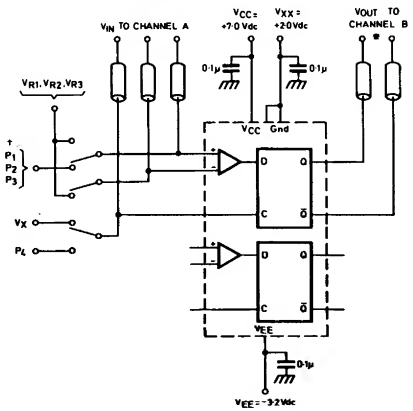
NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| = 12$ Vdc.

② Unused clock inputs may be tied to ground

③ See Figure 10

④

All Temperatures	V_{R2}	V_{R3}
SP1650	+4.900	-0.400
SP1651	+4.400	-0.900



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

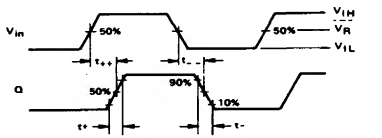
†Refer to Fig. 4 for input pulse definitions.

* Complement of output under test should always be loaded with 50ohms to ground

Fig. 3 Switching time test circuit at +25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

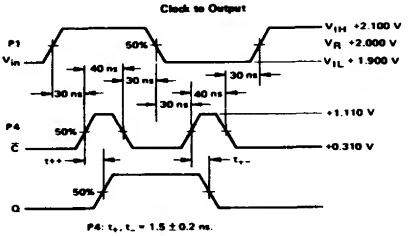


Test pulses: t_+, t_- = 1.5 ±0.2 ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

TEST PULSE LEVELS

	Pulse 1		Pulse 2		Pulse 3	
	SP1650	SP1651	SP1650	SP1651	SP1650	SP1651
V_{IH}	+2.100V	+2.100V	+5.000V	+4.500V	–0.300V	–0.800V
V_R	+2.000V	+2.000V	+4.900V	+4.400V	–0.400V	–0.900V
V_{IL}	+1.900V	+1.900V	+4.800V	+4.300V	–0.500V	–1.000V

Clock to Output



P4: t_+, t_- = 1.5 ±0.2 ns.

Fig. 4 Switching and propagation waveforms @ 25°C

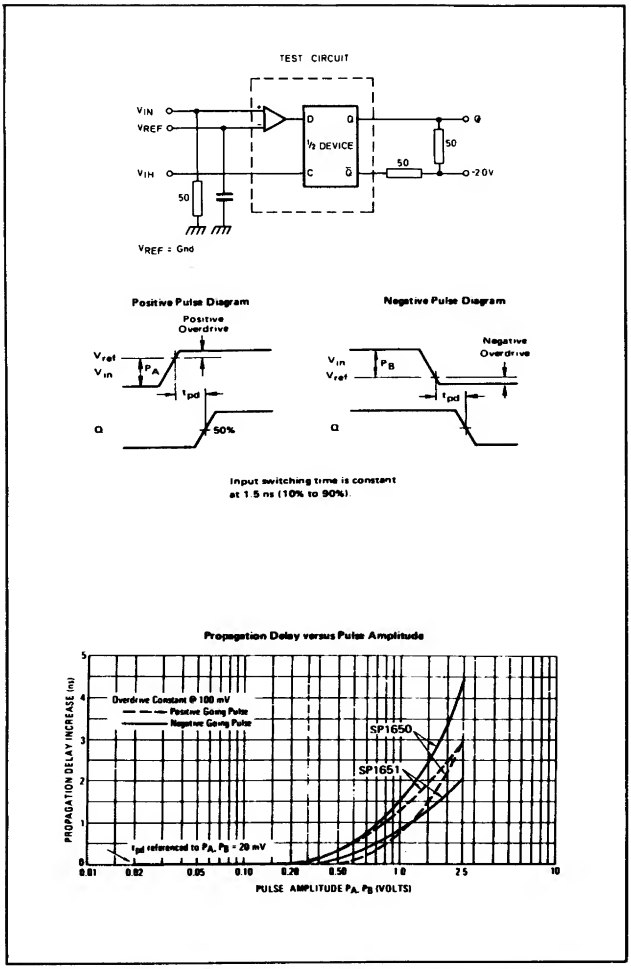


Fig. 5 Propagation delay (t_{pd}) v. input pulse amplitude and constant overdrive

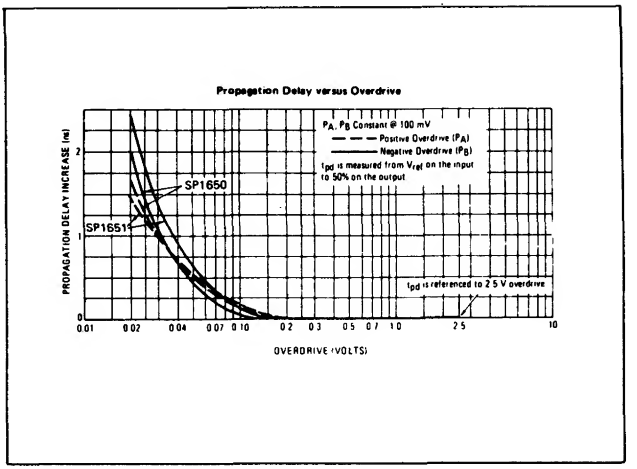


Fig. 5 (continued)

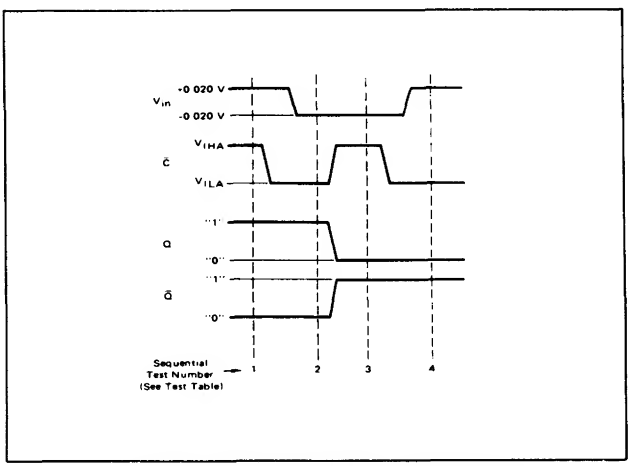


Fig. 6 Logic threshold tests (waveform sequence diagram)

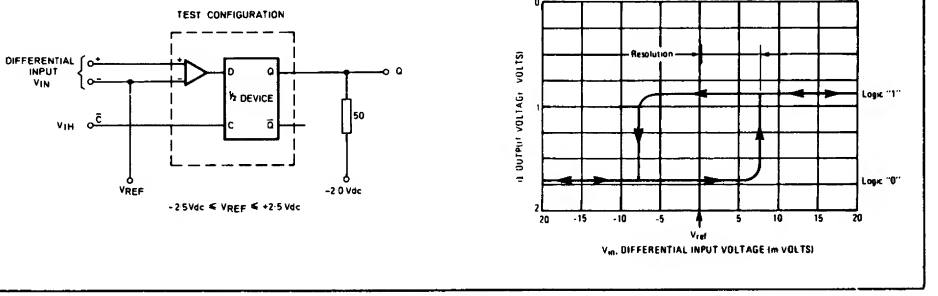


Fig. 7 Transfer characteristics (Q v. Vin)

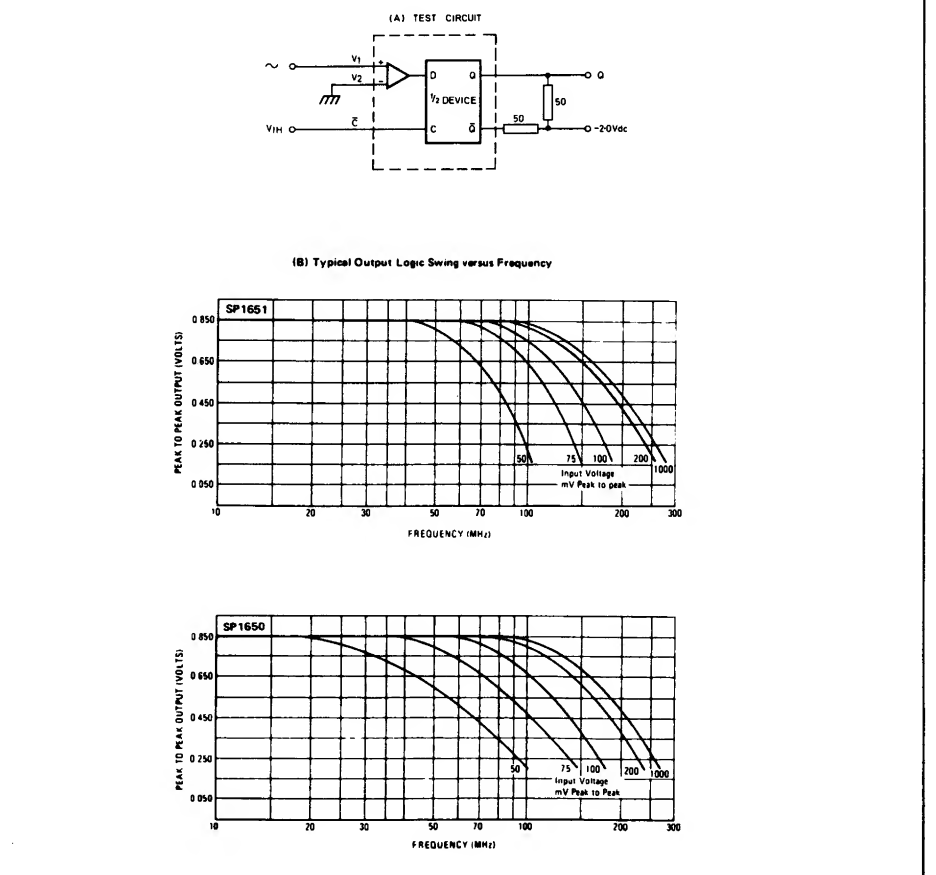
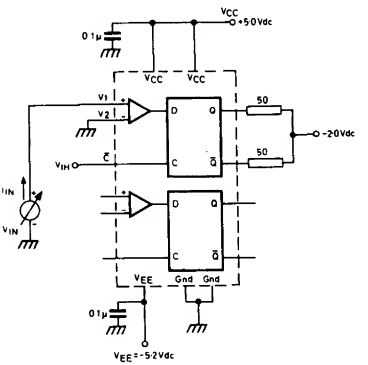
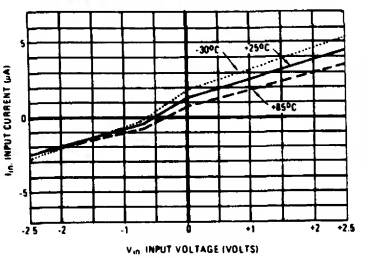


Fig. 8 Output voltage swing v. frequency

TEST CIRCUIT



Typical SP1650 (Complementary Input Grounded)



Typical SP1651 (Complementary Input Grounded)

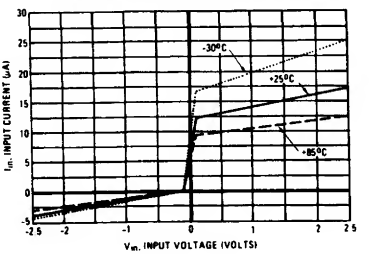
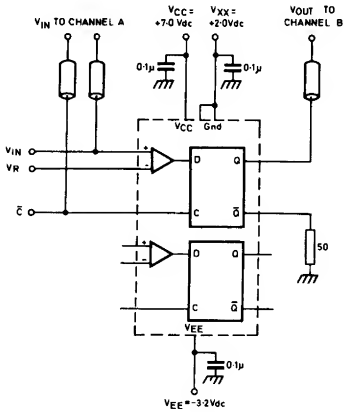


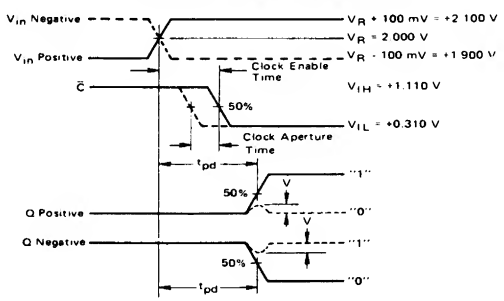
Fig. 9 Input current v. input voltage



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



——— Clock enable time=minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200ps.

----- Clock aperture time=time difference between clock enable time and time that output does not switch and V is less than 150 mV.

Fig. 10 Clock enable and aperture time test circuit and waveforms @ 25°C

PLESSEY
Semiconductors

SP1658

VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with ECL III and ECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

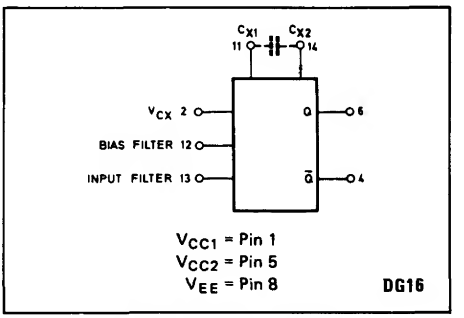


Fig. 1 Block diagram of SP1658

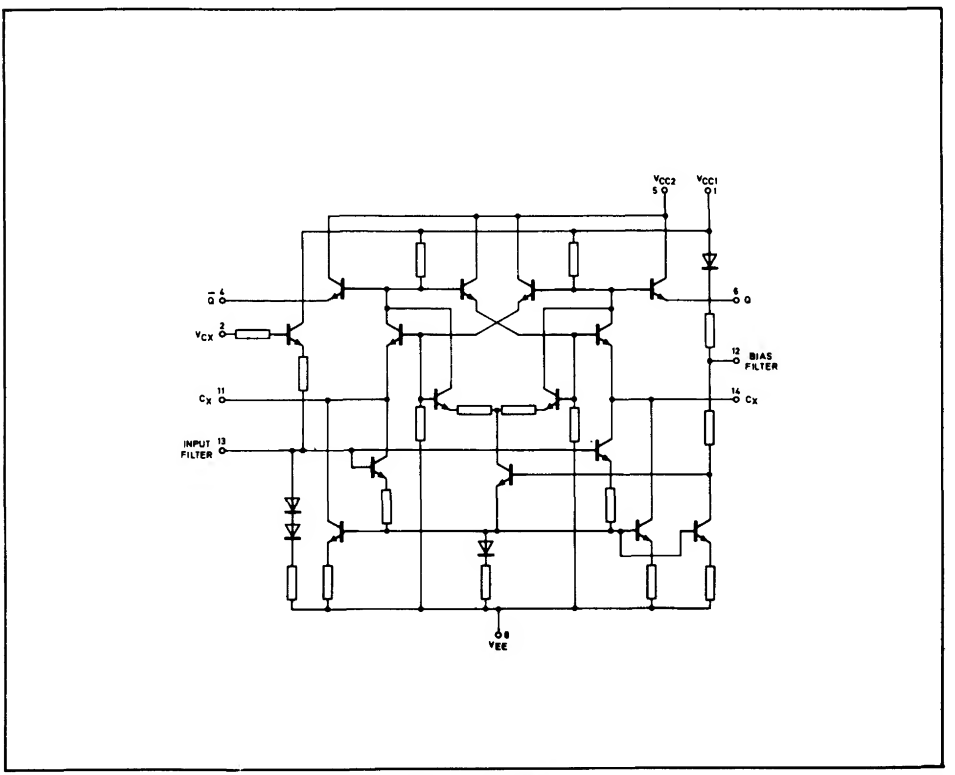


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to --2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1% V_{IH}	V_{IL}	V_3	V_{EE}
-30°C	0.0	-2.0	-1.0	-5.2
+25°C	0.0	-2.0	-1.0	-5.2
+85°C	0.0	-2.0	-1.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1658 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_3	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8*	–	–	–	–	32	–	–	mAdc	2	–	–	8	1,5
		8**	–	–	–	–	32	–	–	mAdc	2	–	–	8	1,5
Input Current	I_{inH}	2*	–	–	–	–	350	–	–	µAdc	2	–	–	8	1,5
Input Leakage Current	I_{inL}	2*	–	–	-0.5	–	–	–	–	µAdc	–	2	–	8	1,5
High Output Voltage $\overline{IOO}$	V_{OH}	4**	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	8	1,5
		6*	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	8	1,5
Low Output Voltage $\overline{IOO}$	V_{OL}	4*	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	8	1,5
		6**	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	V_{CX} +2.0 V	V_{EE} -3.2 V	V_{CC} +2.0 V
Rise Time (10% to 90%)	t_+	6	–	3.6	–	–	3.5	–	3.8	ns	–	11,14	2	8	1,5
Fall Time (10% to 90%)	t_-	6	–	3.1	–	–	3.0	–	3.3	ns	–	11,14	2	8	1,5
Oscillator Frequency	f_{osc1}	–	130	–	130	155	190	110	–	MHz	–	11,14	2	8	1,5
	f_{osc2}	–	–	–	78	90	120	–	–	MHz	11,14	–	2	8	1,5
Tuning Ratio Test †	TR	–	–	–	3.1	4.5	–	–	–	–	11,14	–	–	8	1,5

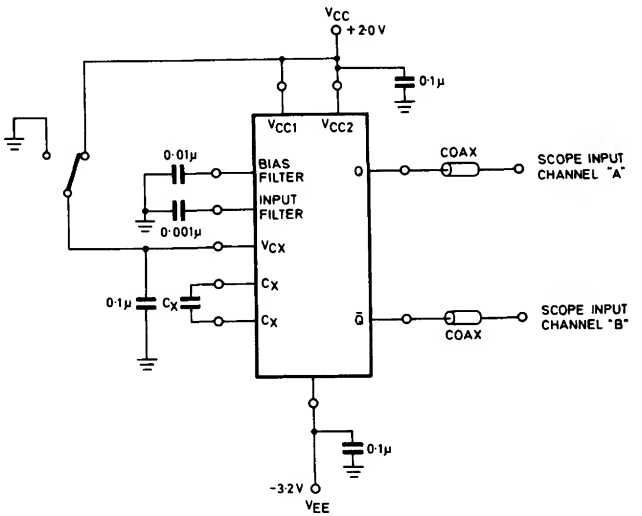
*Germanium diode (0.4 drop) forward biased from 11 to 14 (11 —▶|— 14)

**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 —|◀— 14)

†$TR = \frac{\text{Output frequency at } V_{CX} = +2.0\text{ V}}{\text{Output frequency at } V_{CX} = \text{Gnd}}$

CX1 = 10pF connected from pin 11 to pin 14

CX2 = 5pF connected from pin 11 to pin 14



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{2}$ inch from TP_{in} to input pin and TP_{out} to output pin.

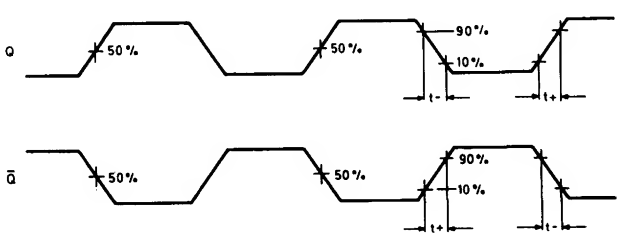


Fig. 3.Switching time test circuit and waveforms

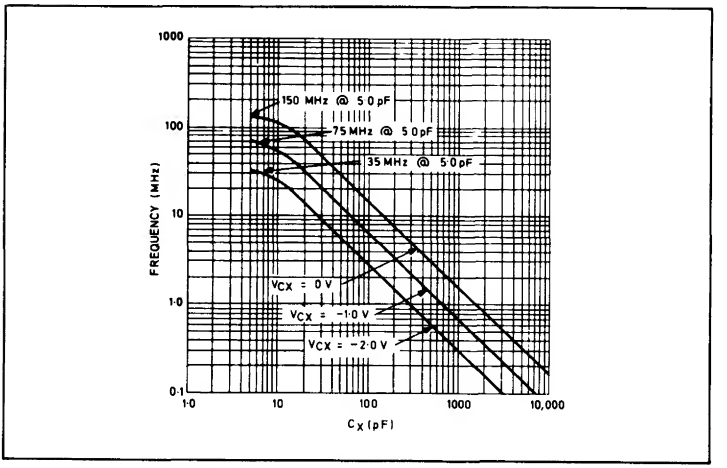


Fig.4 Output frequency v capacitance for three values of input voltage

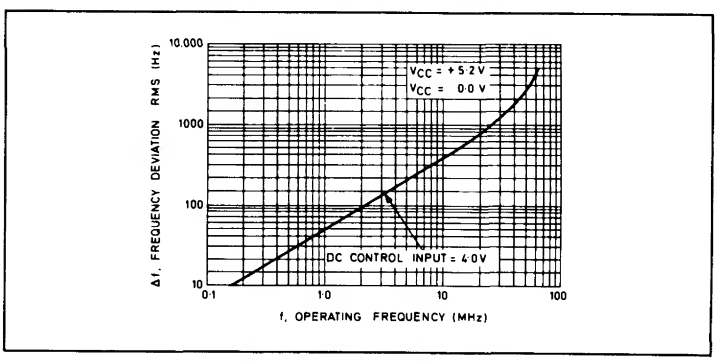


Fig.5 RMS noise deviation v operating frequency

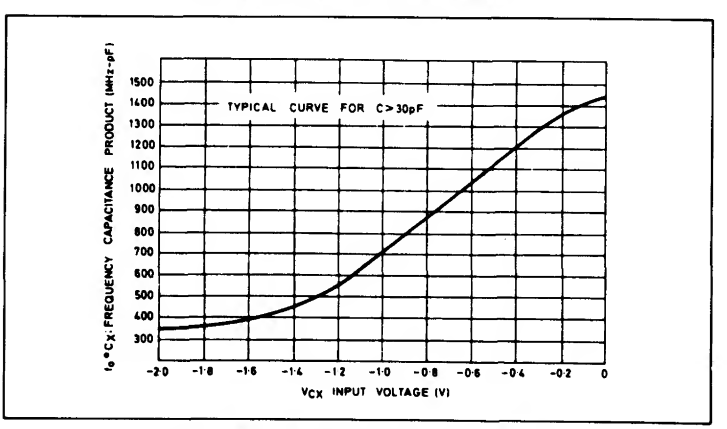


Fig.6 Frequency-capacitance product v control voltage V_{CX}

PLESSEY
Semiconductors

SP1660

DUAL 4-INPUT OR/NOR GATE

SP1660 provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (-30°C to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

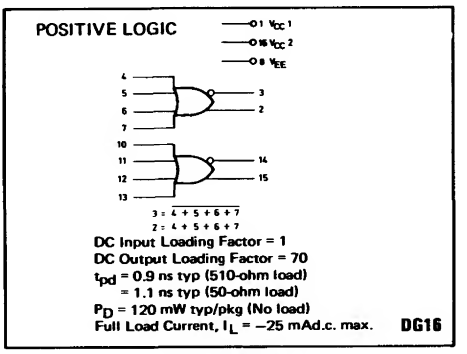


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

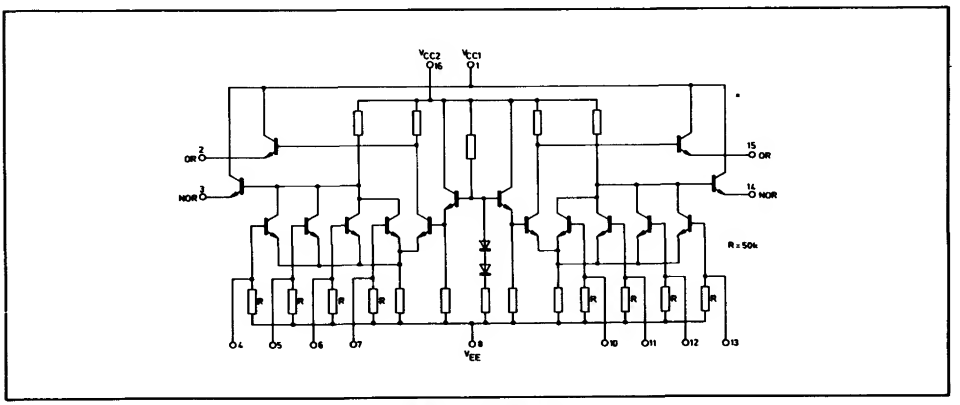


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	µAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
NOR Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "1" Threshold Voltage	V_{OHA}	3	-1.085	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic "1" Threshold Voltage	V_{OHA}	2	-1.085	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9			2				
	t_{4+2+}	2	–	1.6	–	1.5	–	1.7			2	–	–		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	–		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

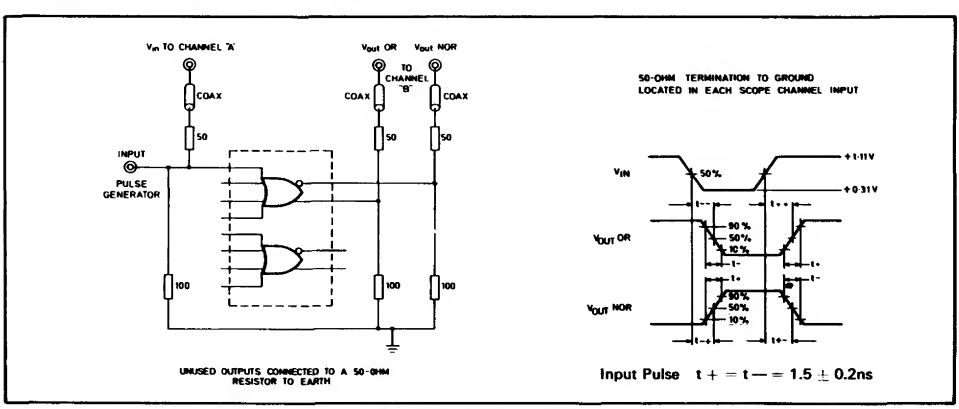


Fig. 3 Switching time test circuit and wave forms at +25° C

PLESSEY
Semiconductors

SP1662

QUAD 2-INPUT NOR GATE

The SP1662 comprises four 2-input NOR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range -30°C to +85°C.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

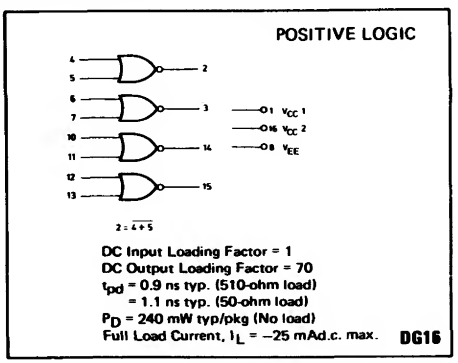


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- ECL 10000—Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	−55°C to +150°C
Junction operating temp.	< +125°C

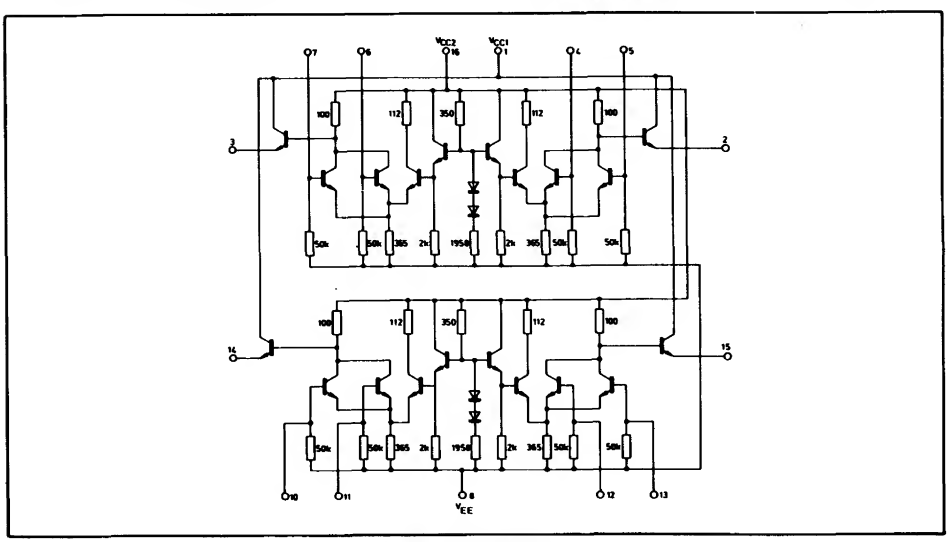


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

Characteristic	Symbol	Pin Under Test	SP1662 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc
Input Current	I_{inH}	*	–	–	–	350	–	–	µAdc
	I_{inL}	*	–	–	0.5	–	–	–	µAdc
Logic '1' Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc
			-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc
Logic '0' Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc
			-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc
Logic '1' Threshold Voltage	V_{OHA}	2	-1.066	–	-0.980	–	-0.910	–	Vdc
			-1.066	–	-0.980	–	-0.910	–	Vdc
Logic '0' Threshold Voltage	V_{OLA}	2	–	-1.830	–	-1.606	–	-1.558	Vdc
		2	–	-1.830	–	-1.606	–	-1.558	Vdc
Switching Times (50 Ω Load) Propagation Delay	t_{+-}	2	–	1.8	–	1.5	–	1.7	ns
	t_{-+}	2	–	1.8	–	1.7	–	1.9	ns
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns

* Individually test each input applying V_{IHA} or V_{IL} to input under test

● Test Temperature

TEST VOLTAGE VALUES (Volts)					
V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	
-0.875	-1.890	-1.190	-1.515	-5.2	-30°C
-0.810	-1.850	-1.095	-1.485	-5.2	+25°C
-0.700	-1.830	-1.025	-1.440	-5.2	+85°C

TEST VOLTAGE APPLIED TO PINS LISTED BELOW					
V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
–	–	–	–	8	1,16
–	–	–	–	8	1,16
–	–	–	–	8	1,16
4	–	–	–	8	1,16
5	–	–	–	8	1,16
4	–	–	–	8	1,16
5	–	–	–	8	1,16
–	–	–	4	8	1,16
–	–	–	5	8	1,16
–	–	4	–	8	1,16
–	–	5	–	8	1,16
Pulse In	Pulse Out			-3.2 V	+2.0 V
4	2	–	–	8	1,16
4	2	–	–	8	1,16
4	2	–	–	8	1,16
4	2	–	–	8	1,16

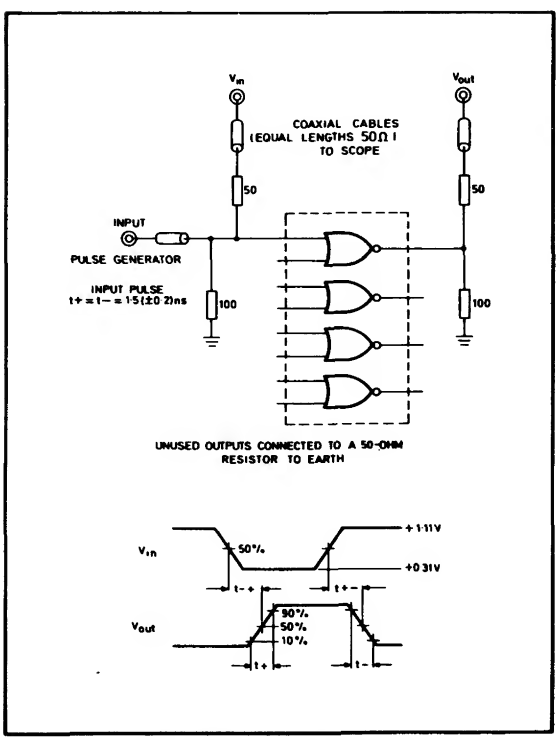


Fig. 3 Switching time test circuit and wave forms at +25°C

PLESSEY
Semiconductors

SP1664

QUAD 2-INPUT OR GATE

The SP1664 comprises four 2-input OR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (-30°C to +85°C).

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

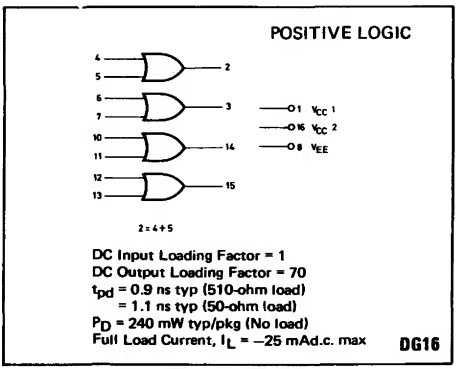


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

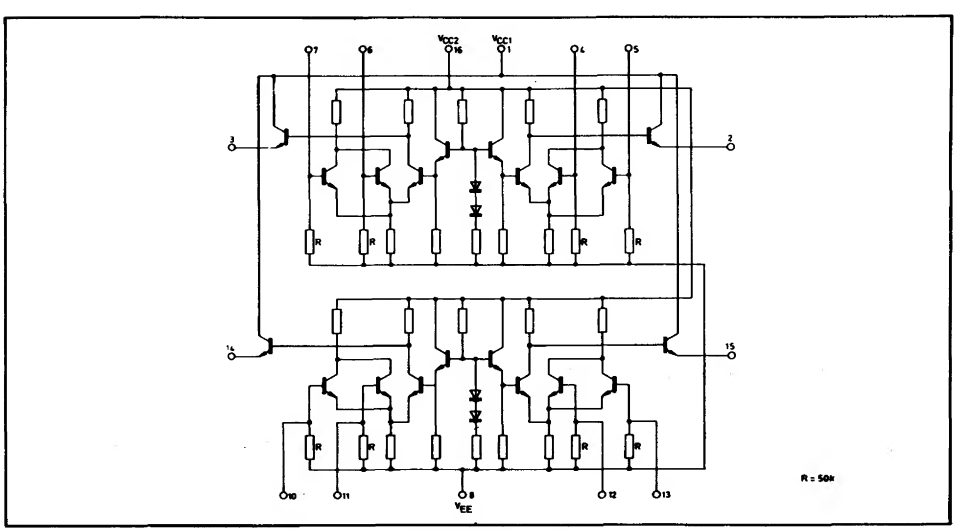


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

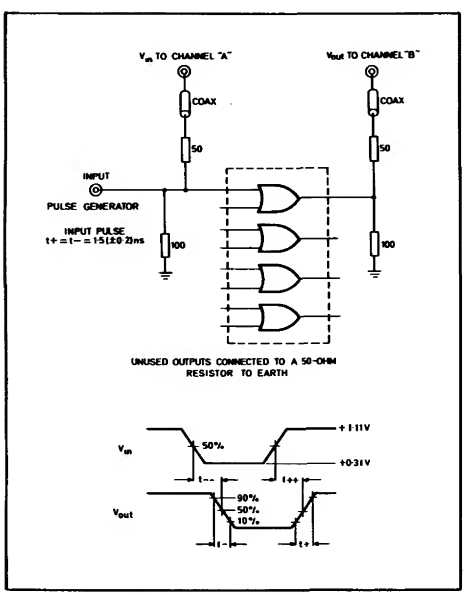


Fig. 3 Switching time test circuit and wave forms at +25°C

Characteristic	Symbol	Pin Under Test	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
TEST VOLTAGE VALUES (Volts)										V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	
@ Test Temperature										-0.875	-1.890	-1.100	-1.515	-5.2	
-30°C										-0.810	-1.850	-1.060	-1.485	-5.2	
+25°C										-0.700	-1.830	-1.025	-1.440	-5.2	
+85°C										TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					
Power Supply Drain Current	I_E	8	-	-	-	56	-	-	mAdc	-	-	-	-	8	1,16
Input Current	$I_{in\,H}$	*	-	-	-	350	-	-	μAdc	*	-	-	-	8	1,16
	$I_{in\,L}$	*	-	-	0.5	-	-	-	μAdc	-	*	-	-	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.980	-0.810	-0.890	-0.700	Vdc	4	-	-	-	8	1,16
		2	-1.045	-0.875	-0.980	-0.810	-0.890	-0.700	Vdc	5	-	-	-	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	-1.620	-1.830	-1.575	Vdc	-	4	-	-	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	-	5	-	-	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.085	-	-0.980	-	-0.910	-	Vdc	-	-	4	-	8	1,16
		2	-1.085	-	-0.980	-	-0.910	-	Vdc	-	-	5	-	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	-	-1.630	-	-1.600	-	-1.555	Vdc	-	-	-	4	8	1,16
		2	-	-1.630	-	-1.600	-	-1.555	Vdc	-	-	-	5	8	1,16
Switching Times 180 Ω Load										Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+2+}	2	-	1.6	-	1.5	-	1.7	ns	4	2	-	-	8	1,16
	t_{4-2-}	2	-	1.6	-	1.7	-	1.9	ns	4	2	-	-	8	1,16
Rise Time	t_{2+}	2	-	2.2	-	2.1	-	2.3	ns	4	2	-	-	8	1,16
Fall Time	t_{2-}	2	-	2.2	-	2.1	-	2.3	ns	4	2	-	-	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test

PLESSEY
Semiconductors

SP1666

DUAL CLOCKED R-S FLIP-FLOP

Two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage.

The device is useful as a high-speed dual storage element.

TRUTH TABLE

S	R	C	Q_{n+1}
∅	∅	0	Q_n
0	0	1	Q_n
1	0	1	0
0	1	1	0
1	1	1	N.D.

∅ = Don't care
N.D. = Not Defined

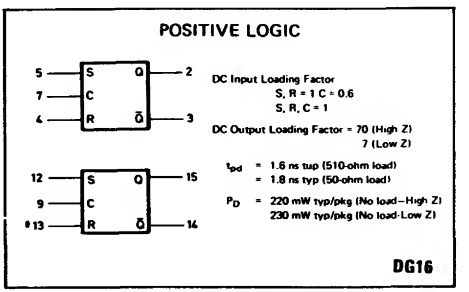


Fig. 1 Logic diagram of SP1666

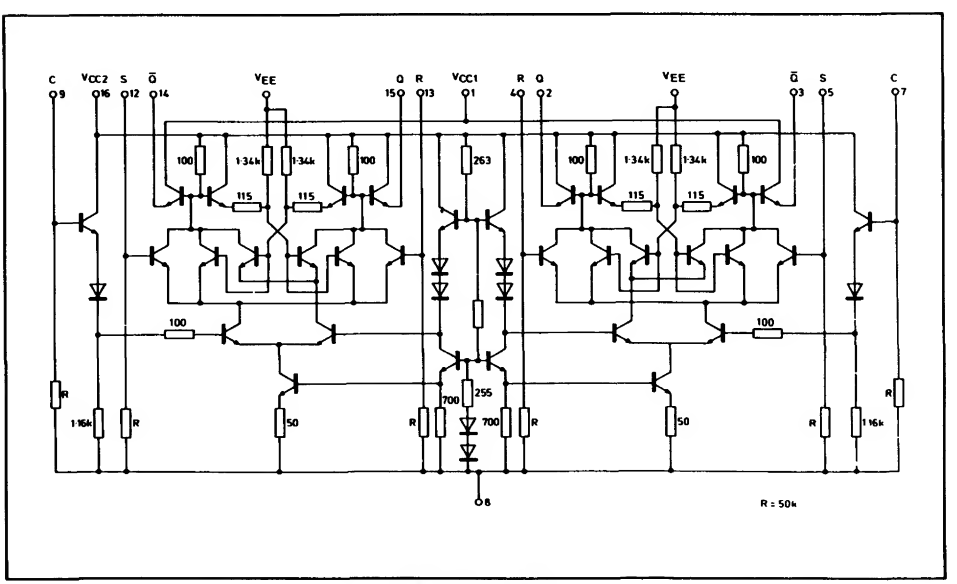


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

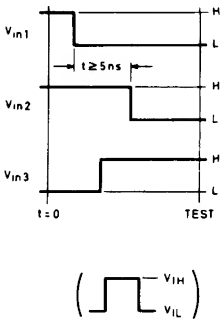
This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.075	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1666 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85 Min	+85 Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	I_{inL}	12	–	–	0.500	–	–	–	µAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	µAdc	–	9,13	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	15 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "1" Output Voltage	V_{OH}	14 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	9	–	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
"$\bar{Q}$" Logic "1" Output Threshold Voltage	V_{OHA}	14 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
"$\bar{Q}$" Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	9	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{9+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9+15-}	15									15	–	–		
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Set Input	t_{12+15+}	15	1.0	2.5	1.0	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14							ns	12	14	–	–	8	1,16
Reset Input	t_{13+14-}	14							ns	13	14	–	–	8	1,16
	t_{13+15+}	15							ns	13	15	–	–	8	1,16
Rise Time	t_+	14,15	0.8	2.8	0.8	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16

○ Notes appear on page following Electrical Characteristics tables

(1) I_E is measured with no output pull-down resistors.



(2) Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} ro S (V_{IH} to V_{IL})

(3) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IL} to V_{IL})

(4) Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

(5) Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

(6) Apply V_{in3} to C (V_{IH} to V_{IL})

(7) Apply V_{in3} to S (V_{IH} to V_{IL})

Fig. 3 Notes referred to in electrical characterstics

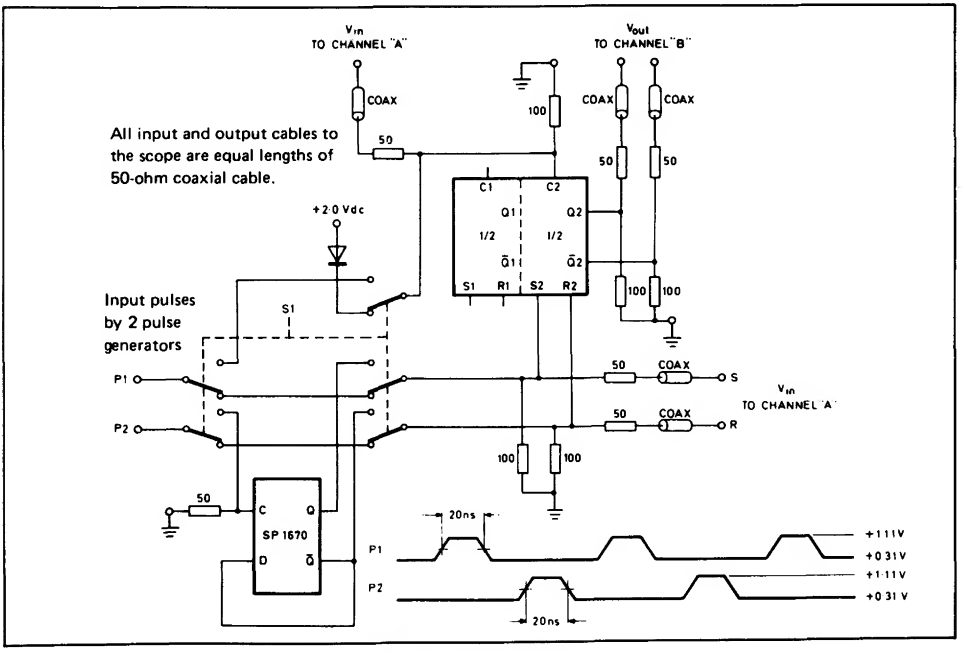


Fig. 4 Switching time test circuit

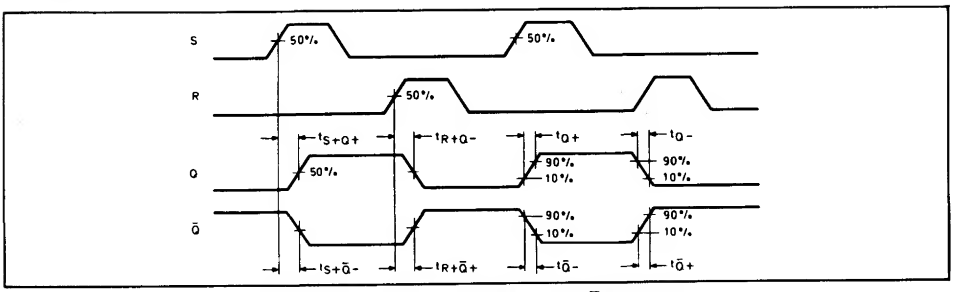


Fig. 5 Switching time waveforms (set/reset to Q/$\bar{Q}$, switch S1 in position shown in Fig. 4)

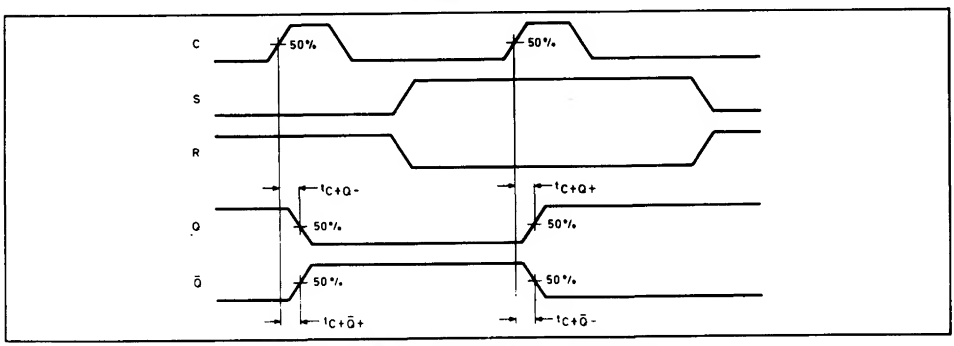


Fig. 6 Switching time waveforms (clock to Q/$\bar{Q}$, switch S1 in opposite position to that shown in Fig. 4)

PLESSEY
Semiconductors

SP1668

DUAL CLOCKED LATCH

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output stage. Whenever the Clock is high, the output follows the data (D) input.

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ø	0	Q_n
1	0	ø	0	1
0	1	ø		
1	1	ø	0	**
ø	ø	0	1	0
ø	ø	1	1	1

** Output stage not defined
ø Don't care

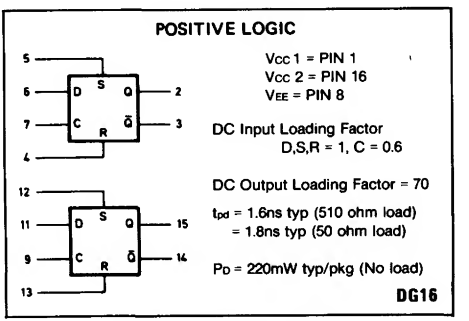


Fig.1 Logic diagram of SP1668

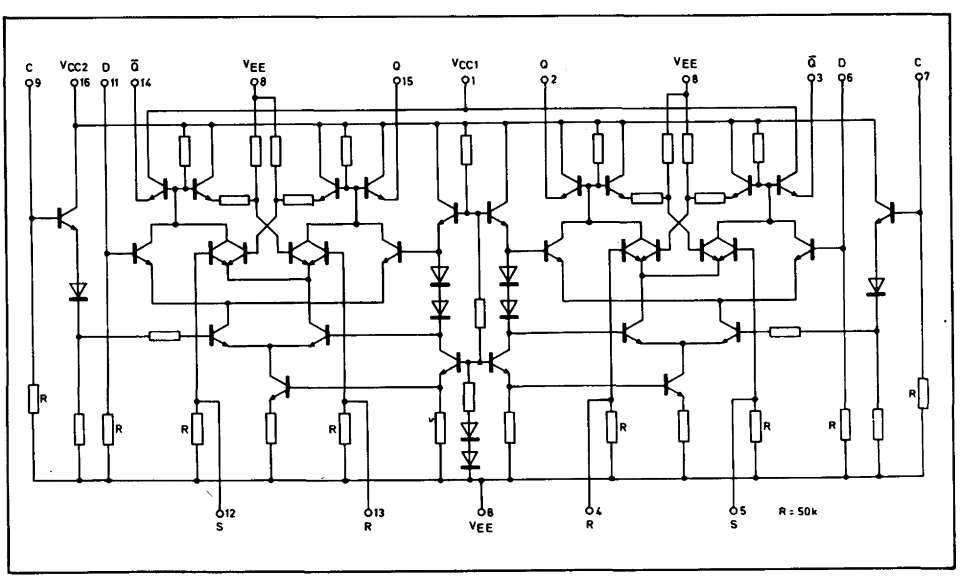


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

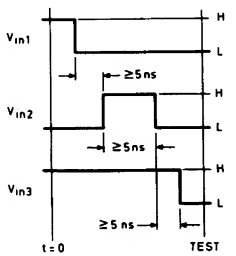
@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1668 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E (Hi Z) 1	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	$I_{in\ H}$	11,12,13②	–	–	–	0.370	–	–	mAdc	11,12,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	11,12,13②	–	–	0.500	–	–	–	µAdc	–	11,12,13	–	–	8	1,16
		9	–	–	0.500	–	–	–	µAdc	–	9	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15③	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Logic	V_{OL}	15⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "1" Output Voltage	V_{OH}	14⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "0" Output Voltage	V_{OL}	14③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15⑦	↓	–	↓	–	↓	–	↓	–	–	11	–	↓	↓
		15⑤		–		–		–		11	–	9	–		
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
		15⑥	–	↓	–	↓	–	↓	↓	–	–	–	11	↓	↓
		15③	–		–		–			–	11	9	–		
"$\bar{Q}$" Logic "1" Output Threshold Voltage	V_{OLA}	14	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
		14⑥	↓	–		–	↓	–	↓	–	–	–	11	↓	↓
		14③		–		–		–		–	11	9	–		
"$\bar{Q}$" Logic "0" Output Threshold Voltage	V_{OLA}	14	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14⑦	–	↓	–	↓	–	↓	↓	–	–	11	–	↓	↓
		14⑤	–		–		–			–	–	9	–		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{9+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9+15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	15	–	–	↓	↓
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Rise Time	t_+	14,15	0.8	2.8	0.9	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16
Set Input	t_{12+15+}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	14	–	–	8	1,16
Reset Input	t_{13+14+}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	14	–	–	8	1,16
	t_{13+15-}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	15	–	–	8	1,16

○Notes appear on page following Electrical Characteristics tables

(1) I_E is measured with no output pulldown resistors.

(2) Test voltage applied to pin under test.



(3) Apply V_{in1} to S (V_{IH} to V_{IL}).

(4) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH} V_{IL})
V_{in3} to D (V_{IH} to V_{IL})

(5) Apply V_{in1} to R (V_{IH} to V_{IL})

(6) Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to C (V_{IH} V_{IL})

(7) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH} V_{IL})

Fig. 3 Notes referred to in electrical characteristics

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Input pulses by 2 pulse generators

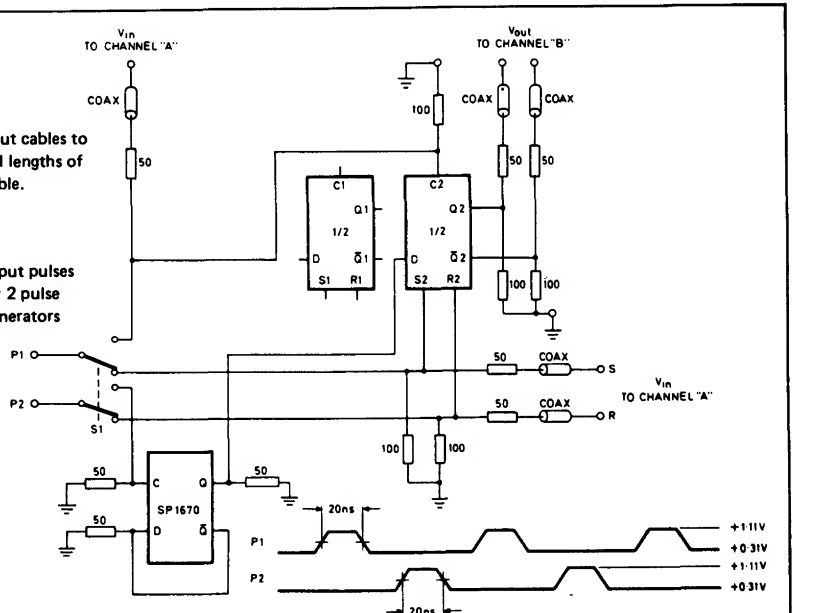


Fig. 4 Switching time test circuit

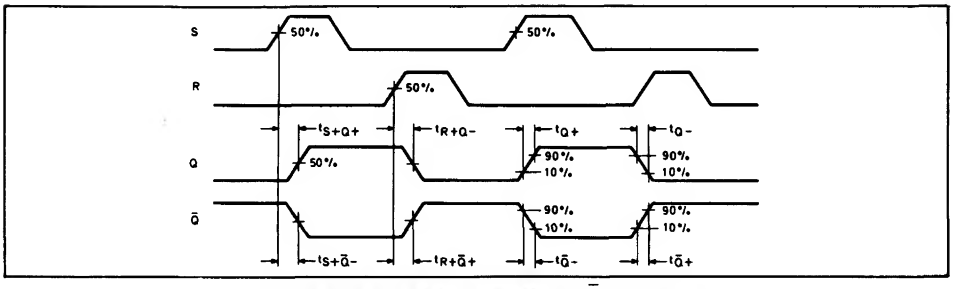


Fig. 5 Switching time waveforms (set/reset to Q/$\bar{Q}$, switch S1 in position shown in Fig. 3)

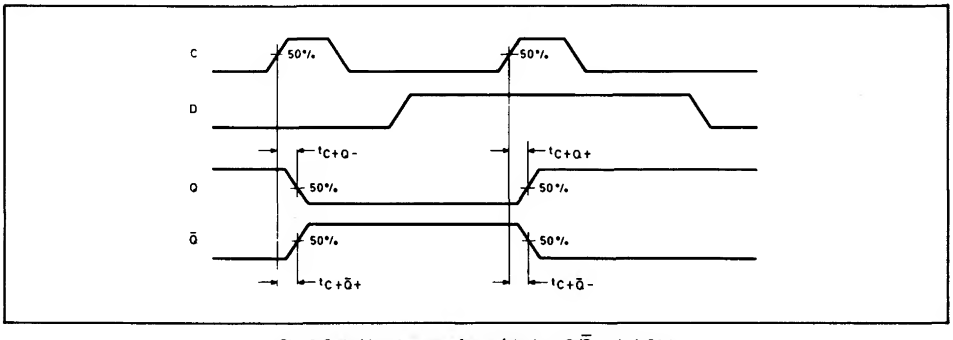


Fig. 6 Switching time waveforms (clock to Q/$\bar{Q}$, switch S1 in position opposite to that shown in Fig. 3

PLESSEY
Semiconductors

SP1670

MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

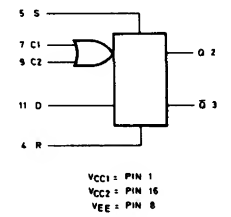
When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



DC Input Loading Factor = C1, C2 = 0.67 D = 0.75 R,S = 1.5
DC Output Loading Factor = 70
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

DG16

Fig. 1 Logic diagram

FEATURES

- Toggle Frequency > 300 MHz
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	⌐	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	⌐	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

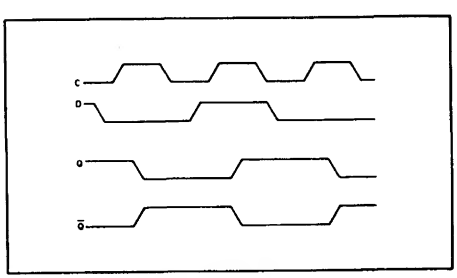


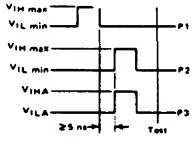
Fig. 2 Timing diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to −2.0 volts.

Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1670 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\,H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	$I_{in\,L}$	4	–	–	0.5	–	–	–	μAdc	9	4	–	–	8	–	–	–	1,16
		5	–	–		–	–	–		9	5	–	–		–	–	–	
		9	–	–		–	–	–		7	9	–	–		–	–	–	
		7	–	–		–	–	–		9	7	–	–		–	–	–	
		11	–	–		–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	11	5,7	–	–	8	9	–	4	1,16
		3	–		–		–			–	4,9,11	–	–		7	–	5	
		2	–		–		–			–	4,7,11	–	–		5	–	9	
		3	–		–		–			11	5,9	–	–		4	–	7	
		2	–		–		–			–	4,7	–	11		5	9	–	
		3	–		–		–			–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay (See Figure 1)	t9+2+	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	8	–	–	–	1,16
	t9+2−	9,2								–	–	–	–		–	–	–	
	t9+3+	9,3								–	–	–	–		–	–	–	
	t9+3−	9,3								–	–	–	–		–	–	–	
Set to Output Delay (See Figure 2)	t5+2+	5,2								–	–	–	–		–	–	–	
	t5+3-	5,3								–	–	–	–		–	–	–	
Reset to Output Delay (See Figure 2)	t4+2-	4,2								–	–	–	–		–	–	–	
	t4+3+	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+,3+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time (See Figure 2)	$t_{2-,3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time (See Figure 3)	t_{S}"1"	2	–	–	–	0.4	–	–		–	–	–	–		–	–	–	
	t_{S}"0"	2	–	–	–	0.5	–	–		–	–	–	–		–	–	–	
Hold Time (See Figure 3)	t_{H}"1"	2	–	–	–	0.3	–	–		–	–	–	–		–	–	–	
	t_{H}"0"	2	–	–	–	0.5	–	–		–	–	–	–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270	–	300	–	270	–	MHz	–	–	–	–		–	–	–	–



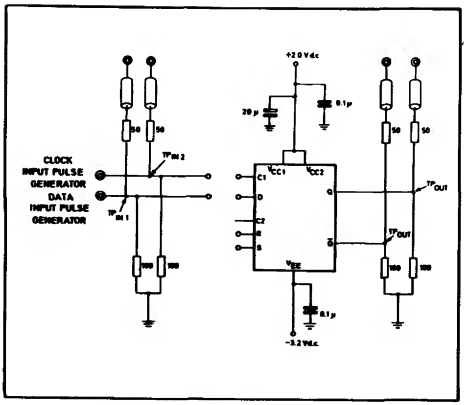


Fig. 3 Propagation delay test circuit

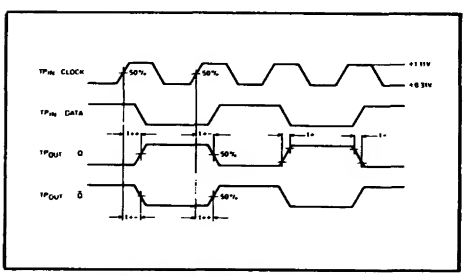


Fig. 4 Clock delay waveforms at +25°C

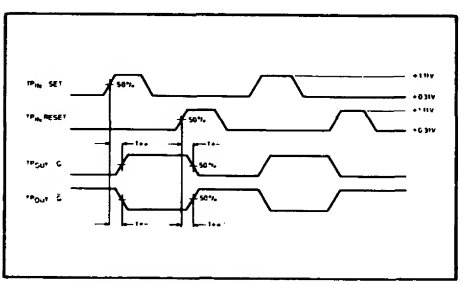


Fig. 5 Set/reset delay waveform at +25°C

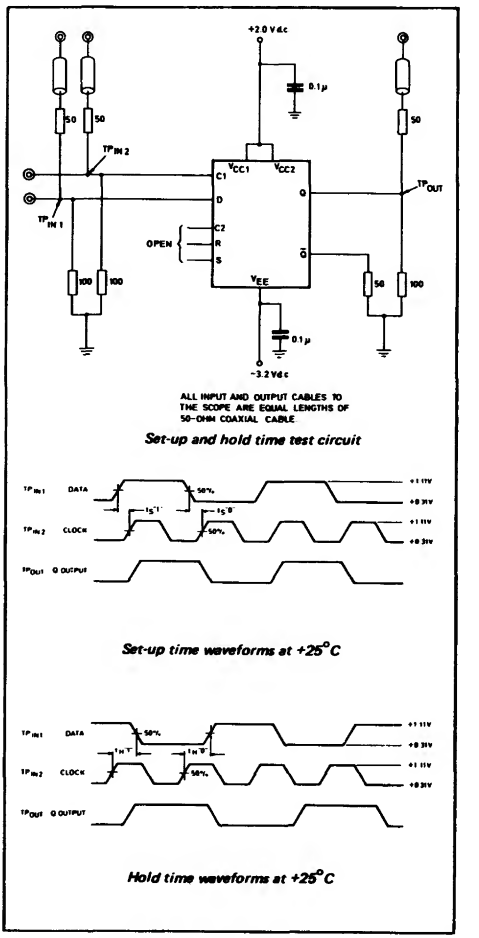


Fig. 6 Set-up and hold time test circuit

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

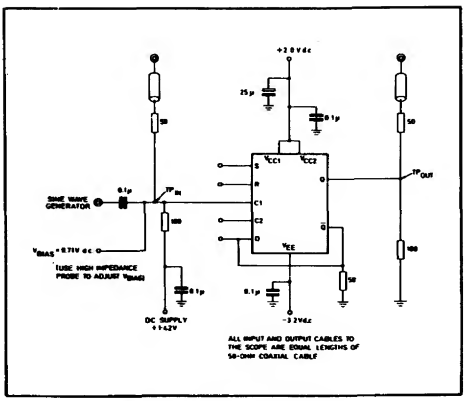


Fig. 7 Toggle frequency test circuit

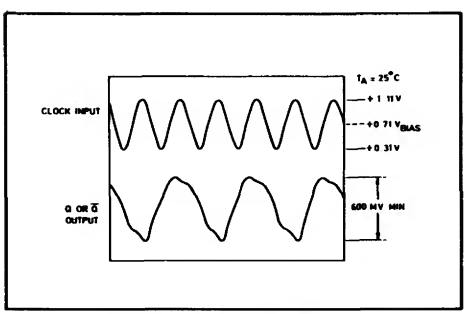


Fig. 8 Toggle frequency waveforms

The maximum toggle frequency of the SP1670 has been exceeded when either:
1. The output peak-to-peak voltage swing falls below 600mV
OR
2. The device ceases to toggle (divide by two). V_{Bias} is defined by the test circuit Fig. 7 and by the waveform in Fig. 8.

Temperature	−30°C	+25°C	+85°C
V_{Bias}	+0.660V	+0.710V	+0.765V

Table 1 Variation of V_{Bias} with temperature

Figures 9 and 10 illustrate minimum clock pulse width recommended for reliable operation of the SP1670

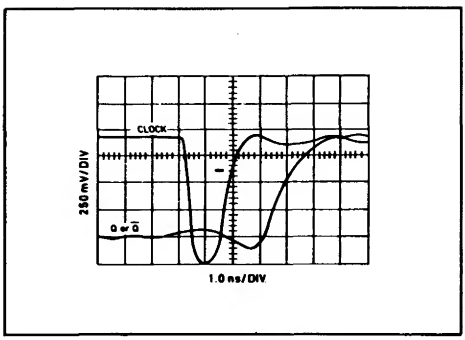


Fig. 9 Minimum 'down time' to clock (Output load = 50Ω)

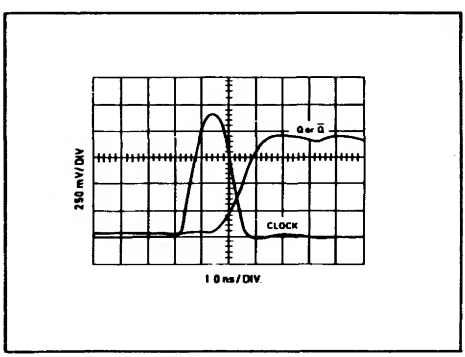


Fig. 10 Minimum 'up time' to clock (Output load = 50Ω)

Operation of the Master-Slave Type D Flip-Flop

In the circuit of Figure 11 assume that initially Q, C, R, S and D are at 0 levels and that $\overline{Q}$ is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7, and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turns on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the $\overline{Q}$ output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

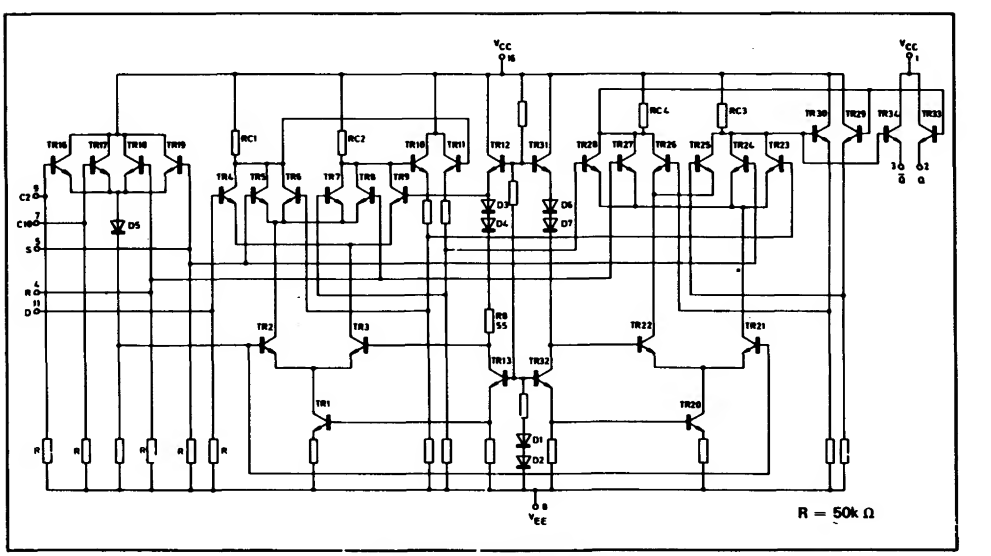


Fig. 11 SP1670 Circuit diagram

PLESSEY
Semiconductors

SP1672

TRIPLE 2-INPUT EXCLUSIVE-OR GATE

This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the centre of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

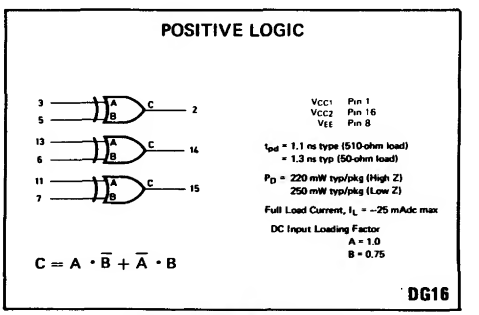


Fig. 1 Logic diagram of SP1672

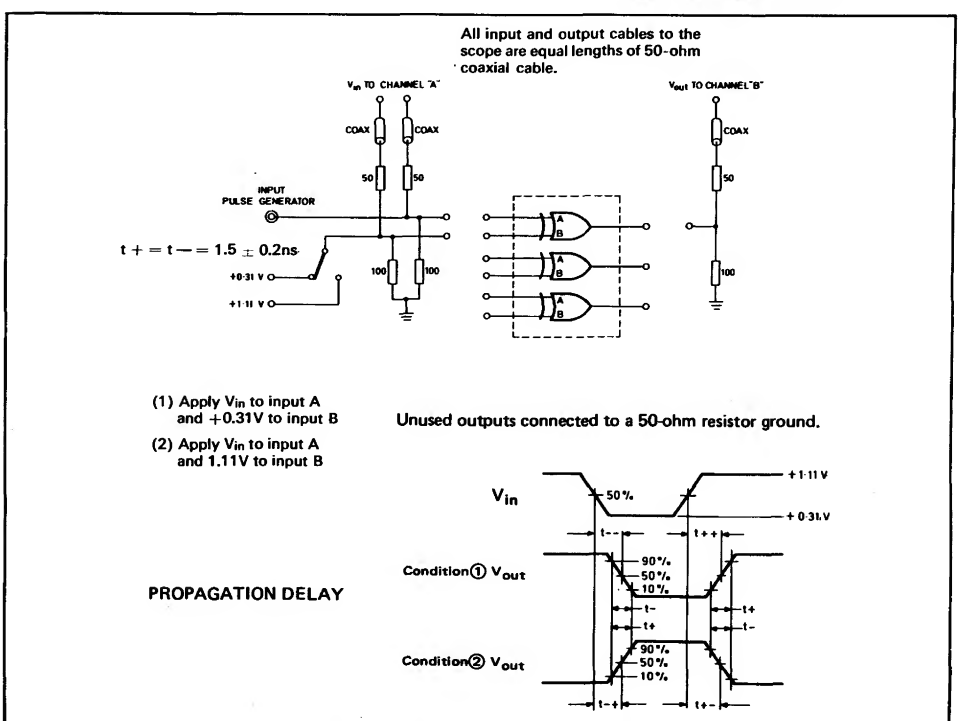


Fig. 2 Switching time test circuit and waveforms at +25°C

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1672 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	$I_{in\ H}$	3,11,13	–	–	–	350	–	–	µAdc	*	–	–	–	8	1,16
	0.75 $I_{in\ H}$	5,6,7	–	–	–	270	–	–	µAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3	5	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	3	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3,5	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	3,5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3	5	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	3	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3,5	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	3,5	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max				Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{2+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

PLESSEY
Semiconductors

SP1674

TRIPLE 2-INPUT EXCLUSIVE-NOR GATE

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the centre of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

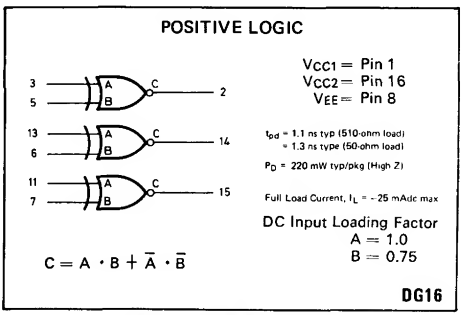


Fig. 1 Logic diagram of SP1674

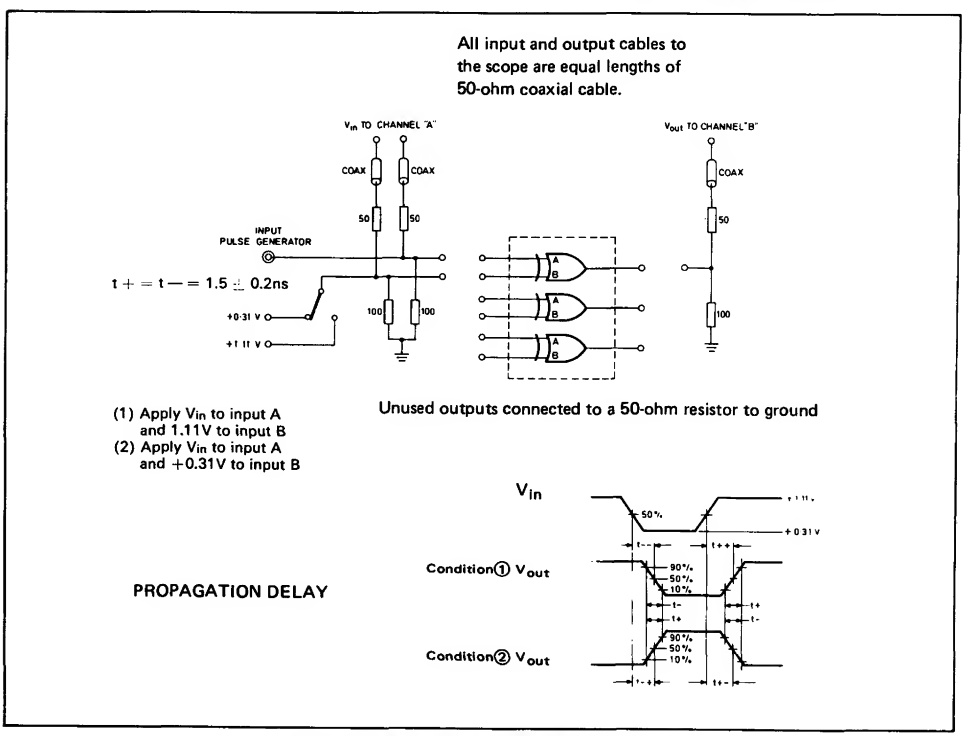


Fig. 2 Switching time test circuit and waveforms at +25°C

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.875	−1.890	−1 180	−1 515	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+85°C	−0.700	−1.830	−1.025	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	SP1674 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	I_{inH}	3,11,13	–	–	–	350	–	–	µAdc	*	–	–	–	8	1,16
	0.75 I_{inH}	5,6,7	–	–	–	270	–	–	µAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3,5	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3	5	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	3	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3,5	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3	5	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	3	8	1,16
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–	↓	↓	↓	↓
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–	↓	–	↓	–	↓		–	–	↓			
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{2+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

PLESSEY
Semiconductors

SP1692

QUAD LINE RECEIVER

Four differential amplifiers with emitter followers, intended for use in sensing differential signals over long lines.

Input pulldown resistors are not provided

A V_{BB} reference voltage is available on pin 9.

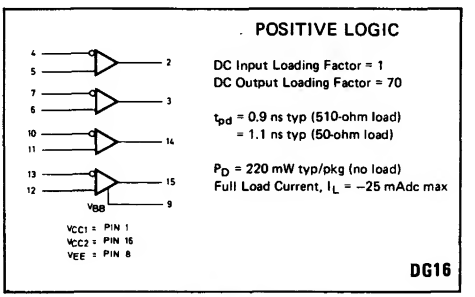


Fig. 1 Logic diagram of SP1692

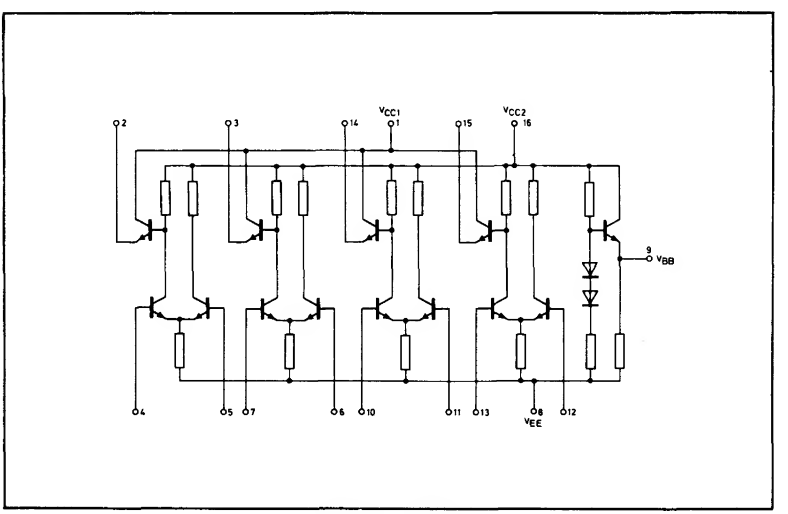


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES					
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
−30°C	-0.875	-1.890	-1.180	-1.515	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485		-5.2
+85°C	-0.700	-1.830	-1.025	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	SP1692 Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						
			−30°C		+25°C		+85°C									
			Min	Max	Min	Max	Min	Max	Unit	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	µAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	µAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	6	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out			−3.2	+2.0
Propagation Delay	t_{4-2+}	2	–	1.6	–	1.5	–	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	–	1.8	–	1.7	–	1.9	↓	↓		↓		↓	↓	↓
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3								
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3								

PLESSEY
Semiconductors

SP16F60

DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (—30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to VEE.

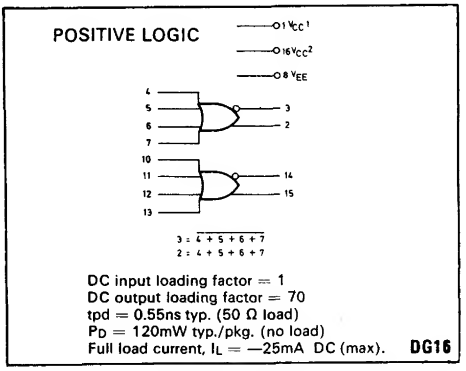


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible with SP1660

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | Vcc - VEE |	8V
Base input voltage	OV to VEE
O/P source current	<40mA
Storage temperature	—55°C to +150°C
Junction operating temperature	<+125C

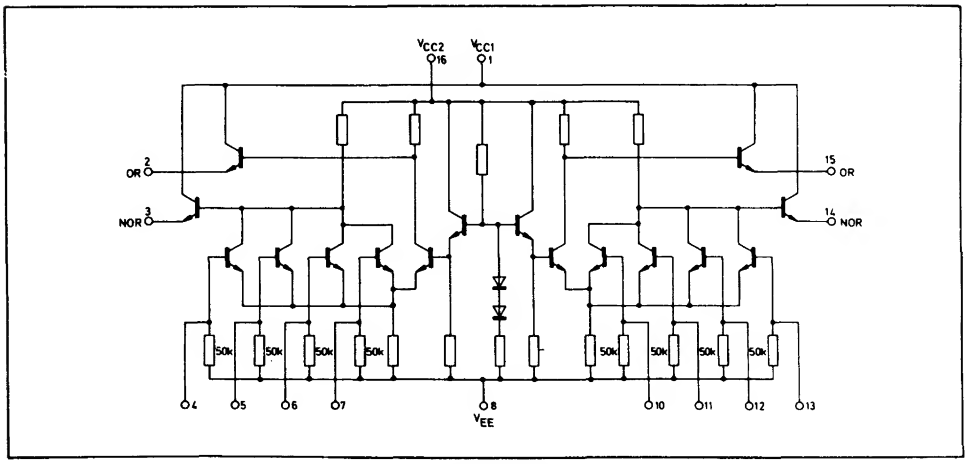


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (V) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	−0.875	−1.890	−1.180	−1.515	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+85°C	-0.700	−1.830	−1.025	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	–	0.55	0.8	–	–	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	–			–	–			2	–	–		
	t_{4+2+}	2	–	–			–	–			2	–	–		
	t_{4-3+}	3	–	–			–	–			3	–	–		
Rise Time 20% to 80%	t_{3+}	3			0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2+}	2			0.35	0.6	–	–	ns	4	2	–	–	8	1,16
Fall Time 20% to 80%	t_{3-}	3			0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2-}	2			0.35	0.6	–	–	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

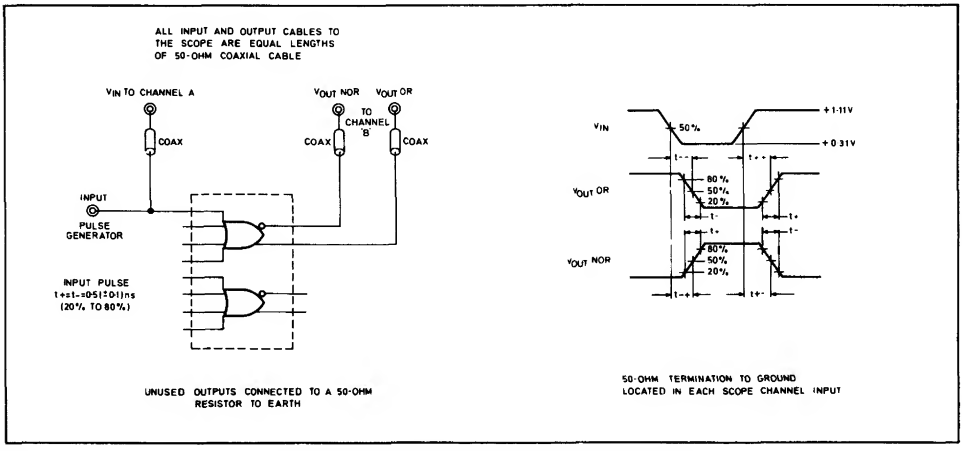


Fig. 3 Switching time test circuit and waveforms at +25°C

PLESSEY
Semiconductors

SP16F70

MASTER/SLAVE D TYPE FLIP-FLOP

The SP16F70 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP16F70 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

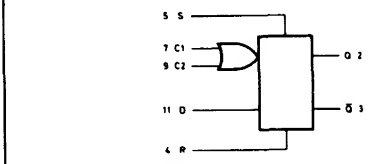
FEATURES

- Toggle Frequency > 350MHz
- ECL 10000 Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

POSITIVE LOGIC



V_{CC} 1 = PIN 1
V_{CC} 2 = PIN 16
V_{EE} = PIN 8

DC Input Loading Factor = C1, C2 = 0.67 D = 0.75 R,S = 1.5
DC Output Loading Factor 70
Power Dissipation = 220mW typical (No Load)
f_{tog} = 350MHz min

DG16

Fig. 1 Logic diagram

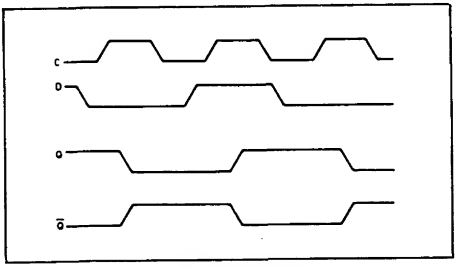


Fig. 2 Timing diagram

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↓	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↓	H
L	L	H	H	Q_n

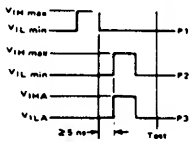
ϕ = Don't Care
ND = Not Defined
C = C1 + C2

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	$I_{in\ L}$	4	–	–	0.5	–	–	–	μAdc	9	4	–	–	8	–	–	–	1,16
		5	–	–		–	–	–		9	5	–	–		–	–	–	
		9	–	–		–	–	–		7	9	–	–		–	–	–	
		7	–	–		–	–	–		9	7	–	–		–	–	–	
		11	–	–		–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	1.600	–	-1.555	Vdc	11	5,7	–	–	8	9	–	4	1,16
		3	–		–		–			–	4,9,11	–	–		7	–	5	
		2	–		–		–			–	4,7,11	–	–		5	–	9	
		3	–		–		–			11	5,9	–	–		4	–	7	
		2	–		–		–			–	4,7	–	11		5	9	–	
		3	–		–		–			–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{9+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	8	–	–	–	1,16
	t_{9+2-}	9,2								–	–	–	–		–	–	–	
	t_{9+3+}	9,3								–	–	–	–		–	–	–	
	t_{9+3-}	9,3								–	–	–	–		–	–	–	
Set to Output Delay	t_{5+2+}	5,2								–	–	–	–		–	–	–	
	t_{5+3-}	5,3								–	–	–	–		–	–	–	
Reset to Output Delay	t_{4+2-}	4,2								–	–	–	–		–	–	–	
	t_{4+3+}	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+,13+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time	$t_{2-,13-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time	$t_{1^{H}1^{H}}$	2	–	–	–	0.4	–	–		–	6	–	–		–	–	–	
	$t_{1^{L}0^{H}}$	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time	$t_{1^{H}1^{L}}$	2	–	–	–	0.3	–	–		–	6	–	–		–	–	–	
	$t_{1^{H}0^{H}}$	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Toggle Frequency	f_{Tog}	2	350	–	350	–	350	–	MHz	–	–	–	–		–	–	–	–



PLESSEY
Semiconductors

SP9131

520 MHz DUAL TYPE D MASTER SLAVE FLIP-FLOP

The SP9131 is a dual master slave type D flip-flop which is pin-for-pin compatible with the ECL10131, but with improved dynamic performance and increased power dissipation.

R-S TRUTH TABLE

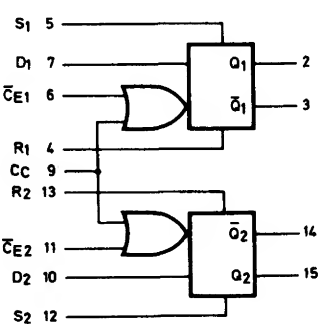
R	S	Q_n+1
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

C	D	Q_n+1
L	ø	Q_n
H	L	L
H	H	H

ø = Don't Care
$C = \overline{C_E} + C_C$.
A clock H is a clock transition from a low to a high state.

$P_D = 364\,mW$
$f_{Tog} = 520\,MHz$ (typ)



VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8

Fig. 1 Logic diagram

ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and a transverse air flow greater than 500 linear FPM is maintained. Outputs are terminated through a 50-ohm resistor to -2.0Volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

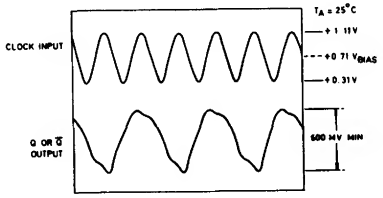
Characteristic	Symbol	Pin Under Test	SP9131 Test Limits −30 C Min	−30 C Max	+25 C Min	+25 C Typ	+25 C Max	+85 C Min	+85 C Max	Unit	TEST VOLTAGE VALUES (Volts) VIH max	VIL min	VIHA min	VILA max	VEE	(Vcc) Gnd
											VOLTAGE APPLIED TO PINS LISTED BELOW:					
Power Supply Current	I_E	8	—	—	—	70	87	—	—	mAdc	—	—	—	—	8	1.16
Input Current	I_{inH}	4	—	—	—	—	600	—	—	µAdc	4	—	—	—	8	1.16
		5	—	—	—	—	600	—	—		5	—	—	—		
		6	—	—	—		300	—	—		6	—	—	—		
		7	—	—	—	—	300	—	—		7	—	—	—		
		9	—	—	—	—	420	—	—		9	—	—	—		
Input Leakage Current	I_{inL}	4,5,*	—	—	0.5	—	—	—	—	µAdc	—	—	—	—	8	1.16
		6,7,9*	—	—	0.5	—	—	—	—	µAdc	—	—	—	—	8	1.16
Logic "1" Output Voltage	V_{OH}	2	-1.06	-0.89	-0.96	—	-0.81	-0.89	-0.70	Vdc	5	—	—	—	8	1.16
		2*	-1.06	-0.89	-0.96	—	-0.81	-0.89	-0.70	Vdc	7	—	—	—	8	1.16
Logic "0" Output Voltage	V_{OL}	3	-1.89	-1.675	-1.85	—	-1.65	-1.825	-1.615	Vdc	5	—	—	—	8	1.16
		3*	-1.89	-1.675	-1.85	—	-1.65	-1.825	-1.615	Vdc	7	—	—	—	8	1.16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.08	—	-0.98	—	—	-0.91	—	Vdc	—	—	5	—	8	1.16
		2*	-1.08	—	-0.98	—	—	-0.91	—	Vdc	—	—	7	9	8	1.16
Logic "0" Threshold Voltage	V_{OLA}	3	—	-1.655	—	—	-1.63	—	-1.595	Vdc	—	—	5	—	8	1.16
		3*	—	-1.655	—	—	-1.63	—	-1.595	Vdc	—	—	7	9	8	1.16
Switching Times Clock Input											+1.11 Vdc		Pulse In	Pulse Out	+3.2Vdc	+2.0Vdc
Propagation Delay	t_{9-2-}	2	—	—		1.0	—	—	—	ns	—	—	9	2	8	1.16
	t_{9-2-}	2	—	—				—	—		7	—	9	2		
	t_{8-2-}	2	—	—				—	—		7	—	6	2		
	t_{6-2-}	2	—	—				—	—		—	—	6	2		
Rise Time (20 to 80%)	t_{2-}	2	—	—		1.0		—	—		7	—	9	2		
Fall Time (20 to 80%)	t_{2-}	2	—	—				—	—		—	—	9	2		
Set Input Propagation Delay	t_{5-2+}	2	—	—		1.0		—	—	ns	—	—	5	2	8	1.16
	t_{12-15+}	15	—	—				—	—		6	—	12	15		
	t_{5-3-}	3	—	—				—	—		—	—	5	3		
	t_{12-14-}	14	—	—				—	—		9	—	12	14		
Reset Input Propagation Delay	t_{4-2-}	2	—	—		1.0		—	—	ns	—	—	4	2	8	1.16
	t_{13-15-}	15	—	—				—	—		6	—	13	15		
	t_{4-3-}	3	—	—				—	—		—	—	4	3		
	t_{13-14-}	14	—	—				—	—		9	—	13	14		
Setup Time	t_{setup}	7	—	—		—	1.0	—	—	ns	—	—	6.7	2	8	1.16
Hold Time	t_{hold}	7	—	—		—	0.2	—	—	ns	—	—	6.7	2	8	1.16
Toggle Frequency (Max)	f_{tog}	2	—	—	520		—	—	—	MHz	—	—	6 *	2	8	1.16

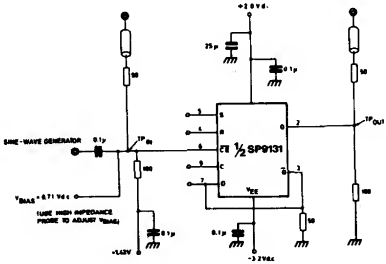
* Test Temperature −30° +25° +85°

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

* Output level to be measured after a clock pulse has been applied to the C_E input (pin 6) $\sqcap\!\_$ $V_{IH\ max}$ / $V_{IL\ min}$

This is advance information and specifications are subject to change without notice.

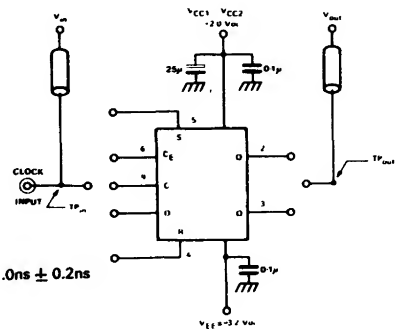




50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

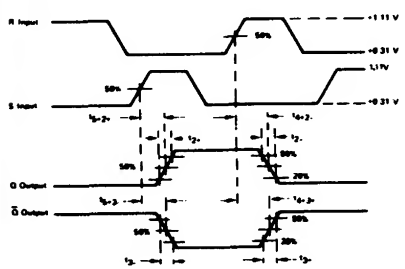
Fig. 2 Toggle frequency test circuit

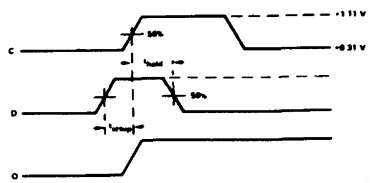


Input Pulse
$t+ = t- = 1.0ns \pm 0.2ns$
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.





NOTE:
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Fig. 3 Switching time test circuit and waveforms at +25°C

PLESSEY
Semiconductors

SP9680

ULTRA FAST COMPARATOR

The SP9680 is an ultra fast comparator manufactured using a high performance bipolar process which makes possible very short propagation delays (2.4ns typ.).

The circuit has differential inputs and complementary ECL outputs, capable of driving 50 Ω lines.

The device is manufactured in a low cost mini-dip package and is intended as an alternative to the faster SP9685 in applications where performance premium and the latch facility are not required.

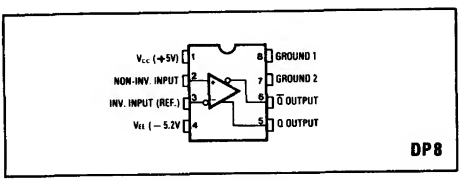


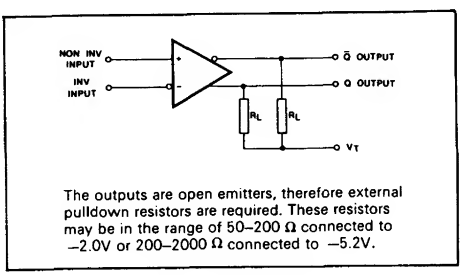
Fig. 1 Pin connections

FEATURES

- Propagation Delay 2.4ns Typ.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- 8-Lead Plastic Package

QUICK REFERENCE DATA

- Supply Voltages +5, −5.2V
- Operating Temperature Range −30°C to +70°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

Fig. 2 Functional diagram

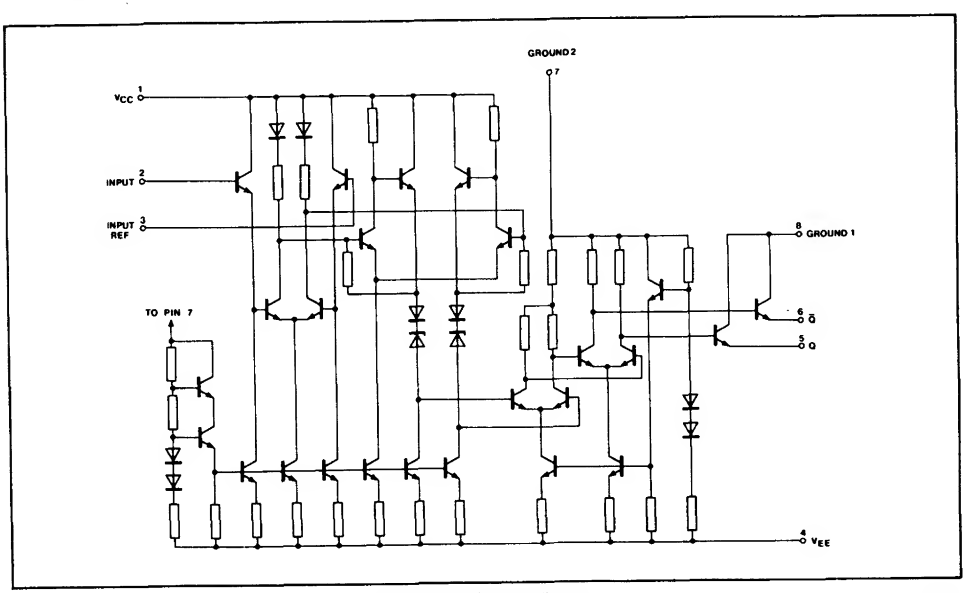


Fig. 3 SP9680 circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C
V_{CC} = 5.00V ± 0.25V
V_{EE} = −5.2V ± 0.25V
R_L = 50 Ω
V_T = −2.0V (See Fig. 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−6		+6	mV	Rs <100 Ω
Input bias current		20	40	µA	
Input offset current			10	µA	
Supply current I_{CC}		18	25	mA	
I_{EE}		22	35	mA	
Total power dissipation		200	300	mW	
Input to Q output delay		2.4	4	ns	} 100mV pulse,10mV overdrive
Input to $\overline{Q}$ output delay		2.4	4	ns	
Common mode range	−2		+2	V	
Common mode rejection ratio		80		dB	
Output logic levels					
Output HIGH	−0.96		−0.81	V	
Output LOW	−1.85		−1.65	V	
Input capacitance		3.5		pF	
Input resistance	50			kΩ	
Operating temperature range	−30		+70	°C	

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage V_{CC} +6V
Negative supply voltage V_{EE} −6V
Output current 30mA
Input voltage ±5V
Differential input voltage ±5V
Storage temperature −55°C to +125°C

PLESSEY
Semiconductors

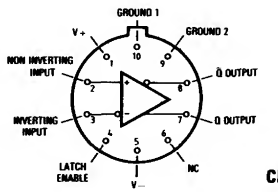
SP9685

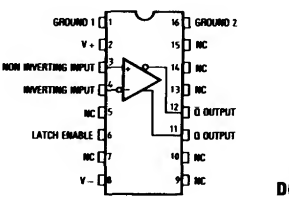
ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50 Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and −5.2V rails.





On metal package, pin 5 is connected to case. On DIP pin 8 is connected to case

Fig. 1 Pin connections

FEATURES

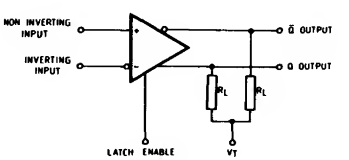
- Propagation Delay 2.2ns typ.
- Latch Set-up Time 1ns max.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM685 – But Faster

QUICK REFERENCE DATA

- Supply voltages +5V, −5.2V
- Operating temperature range −30°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	−6V
Output current	30mA
Input voltage	±5V
Differential input voltage	±5V
Power dissipation	300mW
Storage	−55°C to +150°C
Lead temperature (soldering 60 sec)	300°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V or 200–2000Ω connected to −5.2V

Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{AMB} = 25°C$
$V_{CC} = +5.0V \pm .25V$
$V_{EE} = -5.2V \pm .25V$
$R_L = 50\,\Omega$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	–5		+5	mV	Rs <100 Ω
Input bias current		10	20	μA	
Input offset current			5	μA	
Supply currents Icc		19	23	mA	
IEE		23	34	mA	
Total power dissipation		210	300	mW	
Min. latch set-up time (t_s)		0.5	1	ns	
Input to Q output delay (t_{pd})		2.2	3	ns	100 mV pulse
Input to $\bar{Q}$ output delay (t_{pd})		2.2	3	ns	10 mV overdrive
Latch to Q delay $t_{pd}(E)$		2.5	3	ns	
Latch to $\bar{Q}$ delay $t_{pd}(E)$		2.5	3	ns	
Min. latch pulse width $t_{pw}(E)$		2	3	ns	
Min. hold time (t_h)			1	ns	
Common mode range	–2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			kΩ	
Output logic levels					
Output High	– .96		– .81	V	At nominal supply
Output Low	–1.85		–1.65	V	voltages, see Fig. 4
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

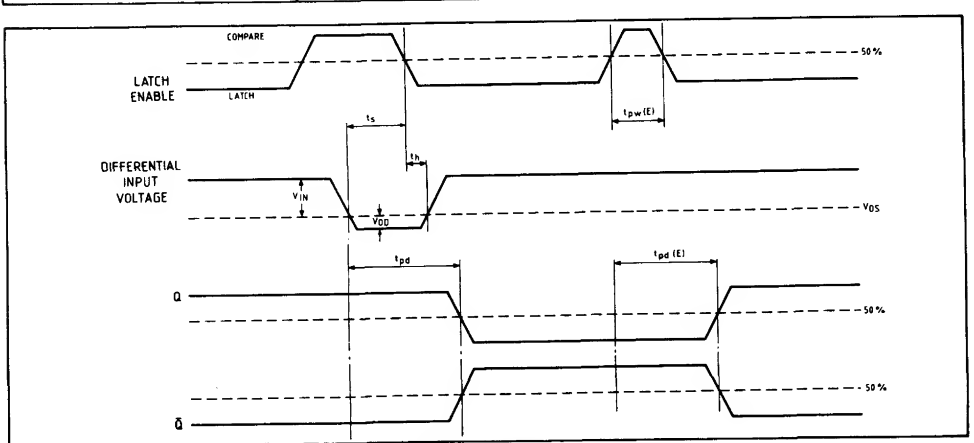


Fig. 3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time tpd. Output Q and $\bar{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Measurement of propagation and latch delays

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.

3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

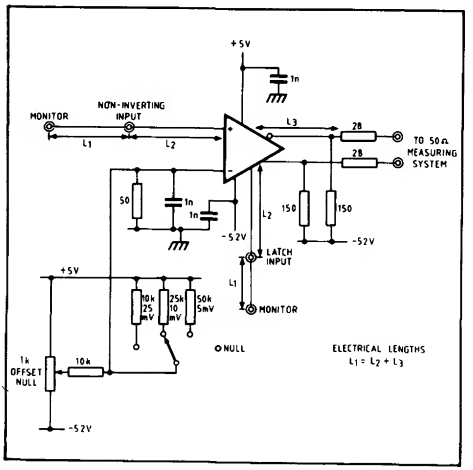


Fig. 4 SP9685 test circuit

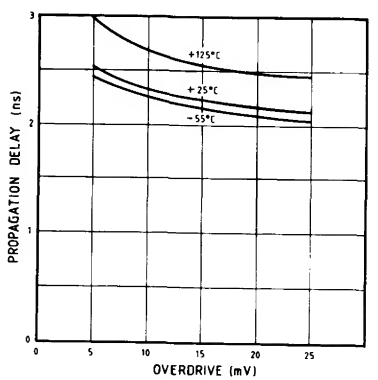


Fig. 6 Propagation delay, latch to output as a function of overdrive

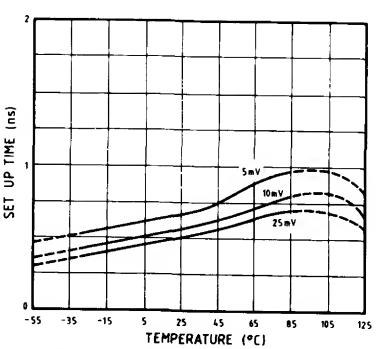


Fig. 8 Set-up time as a function of temperature

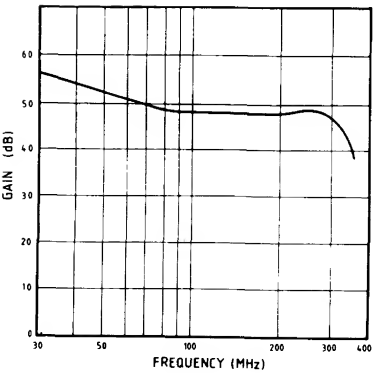


Fig. 5 Open loop gain as a function of frequency

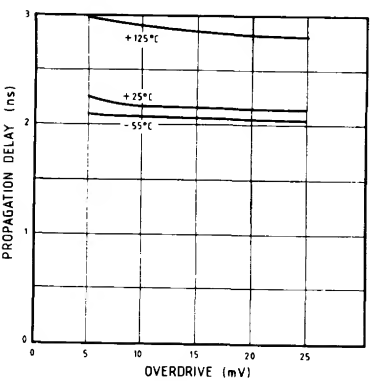


Fig. 7 Propagation delay, input to output as a function overdrive

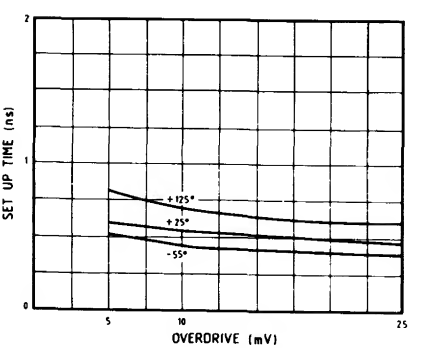


Fig. 9 Set-up time as a function of input overdrive

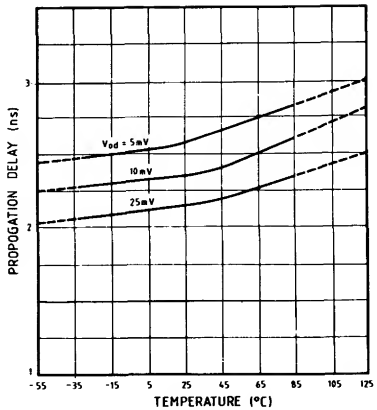


Fig. 10 Propagation delay, input to output as a function of temperature

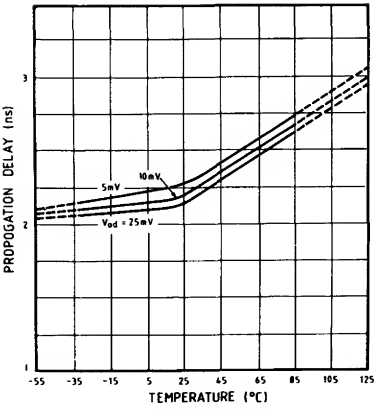


Fig. 11 Propagation delay, latch to output as a function of temperature

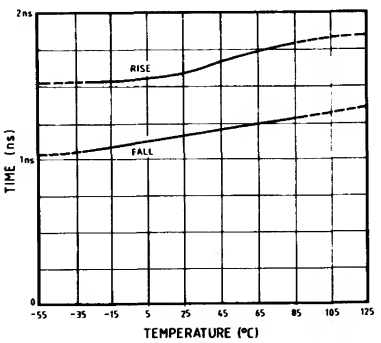


Fig. 12 Output rise and fall times as a function of temperature

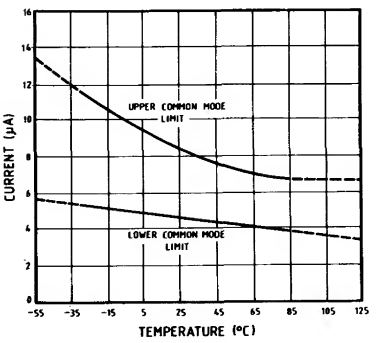


Fig. 13 Input bias currents as a function of temperature

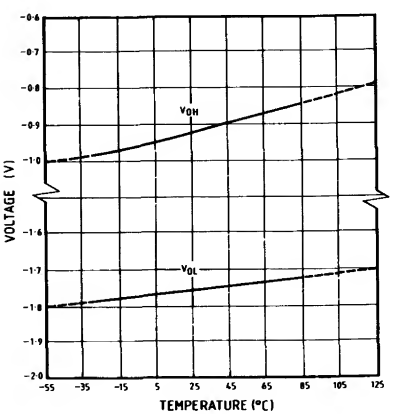


Fig. 14 Output levels as a function of temperature

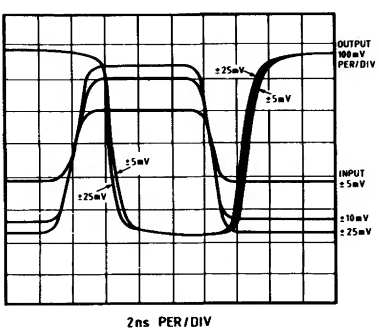


Fig. 15 Response to various input signal levels

PLESSEY
Semiconductors

SP9687

ULTRA FAST DUAL COMPARATOR

The SP9687 is an ultra-fast, dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and $\overline{LE}$ is low, the comparator function is in operation. When LE is driven low and $\overline{LE}$ high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, LE must be connected to ground.

The device is pin compatible with the AM687 and operates from conventional +5V and −5.2V rails.

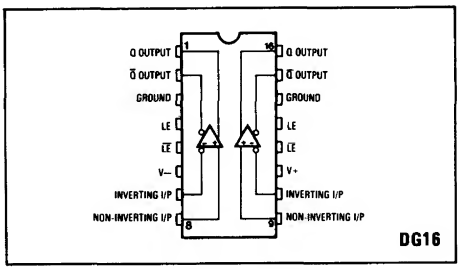
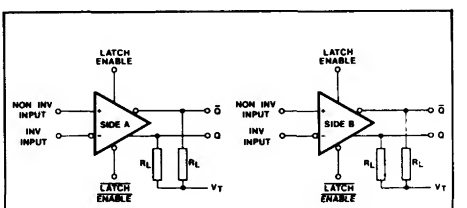


Fig. 1 Pin connections



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

Fig. 2 Functional diagram

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns max.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM687 – But Faster

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	−6V
Output current	30mA
Input voltage	±5V
Differential input voltage	±5V
Power dissipation	590mW
Storage	−55°C to +125°C
Lead temperature (soldering 60 sec)	300°C

QUICK REFERENCE DATA

- Supply voltages +5V, −5.2V
- Operating temperature range −30°C to +85°C

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse, switches the comparator over after a time tpd. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch-falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse with $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$. The $\overline{LE}$ input is omitted for clarity.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{AMB} = 25°C$
$V_{CC} = +5.00V \pm .25V$
$V_{EE} = -5.20V \pm .25V$
$R_L = 50\Omega$
$V_T = -2.0V$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	–5		+5	mV	Rs <100 Ω
Input bias current		5	20	µA	
Input offset current		1	5	µA	
Supply currents Icc		30	46	mA	} Note 3
I_{EE}		54	68	mA	} Nominal conditions
Total power dissipation		430	590	mW	
Min. latch set-up time (t_s)		0.5	1	ns	Notes 1,2
Input to Q output delay (t_{pd})		2.2	3	ns	} 100 mV pulse } note 1
Input to $\overline{Q}$ output delay (t_{pd})		2.2	3	ns	} 10 mV overdrive
Latch to Q delay $t_{pd}(E)$		2.5	3	ns	} Notes 1, 2
Latch to $\overline{Q}$ delay $t_{pd}(E)$		2.5	3	ns	
Min. latch pulse width $t_{pw}(E)$		2	3	ns	
Min. hold time (t_h)			1	ns	
Common mode range	–2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			kΩ	
Output logic levels					
Output High	– .96		– .81	V	At nominal supply
Output Low	–1.85		–1.65	V	voltages
Operating temperature range	–30°		+85°	°C	
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

NOTES
1. These measurements are defined under conditions of a +100mV pulse with –10mV overdrive. The relationship between overdrive and delay is illustrated in Figs. 6 to 8.
2. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.
3. Refers to the entire package. Other data in this table applies to each half device.

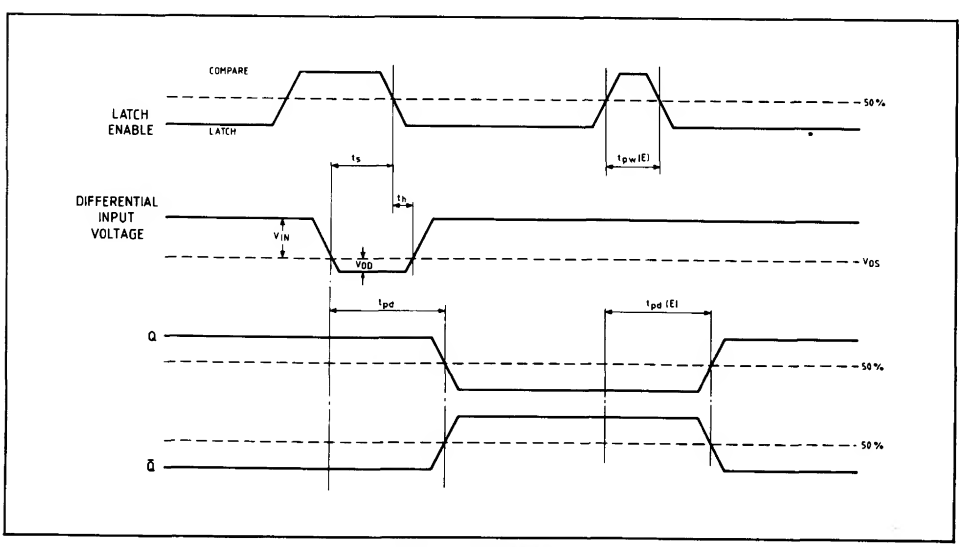


Fig. 3 Timing diagram

PERFORMANCE CURVES

Unless otherwise specified, standard conditions for all curves are $T_{AMB} = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.2V$

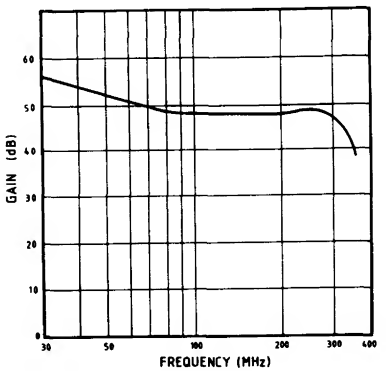


Fig. 4 Open loop gain as a function of frequency

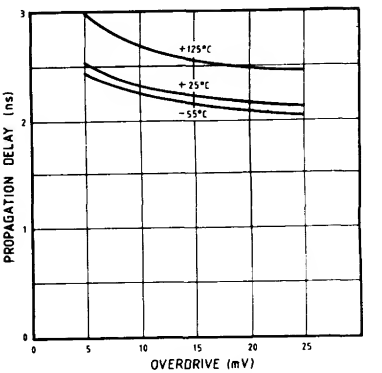


Fig. 5 Propagation delay, latch to output as a function of overdrive

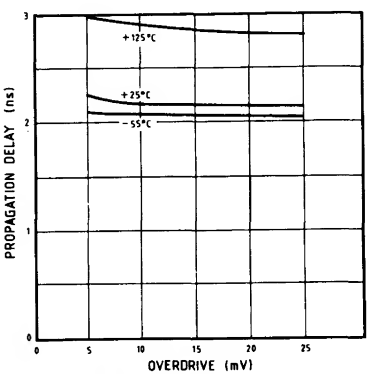


Fig. 6 Propagation delay, input to output as a function of overdrive

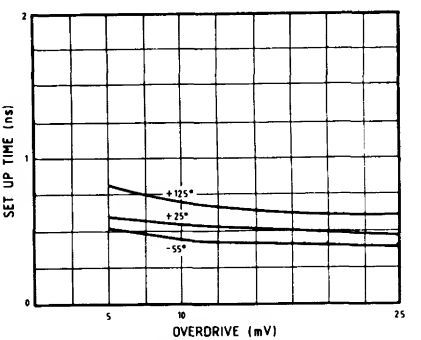


Fig. 7 Set-up time as a function of input overdrive

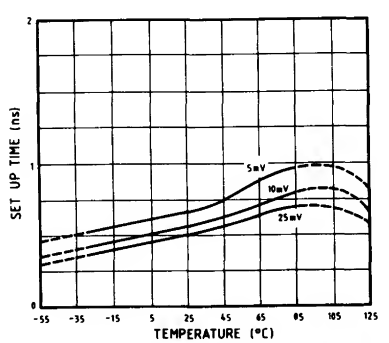


Fig. 8 Set-up time as a function of temperature

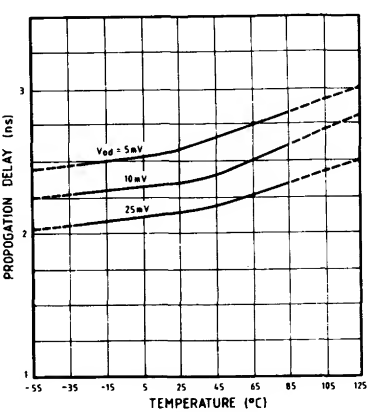


Fig. 9 Propagation delay, input to output as a function of temperature

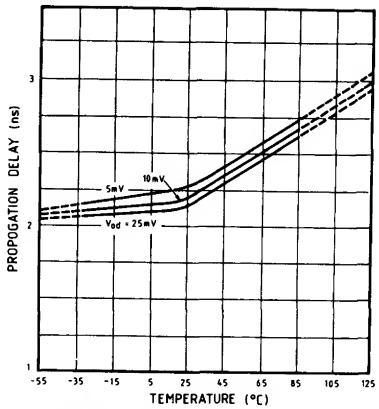


Fig. 10 Propagation delay, latch to output as a function of temperature

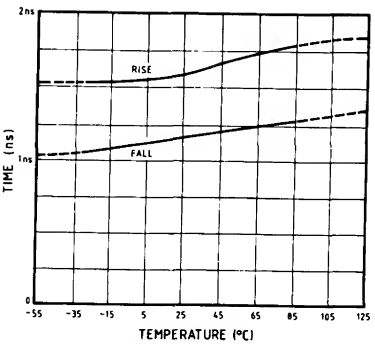


Fig. 11 Output rise and fall times as a function of temperature

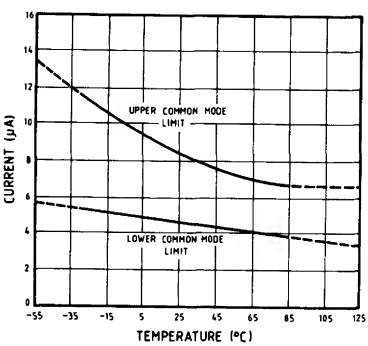


Fig. 12 Input bias currents as a function of temperature

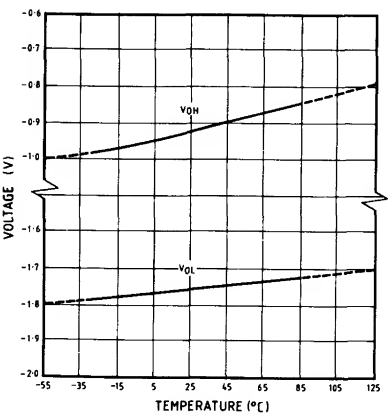


Fig. 13 Output levels as a function of temperature

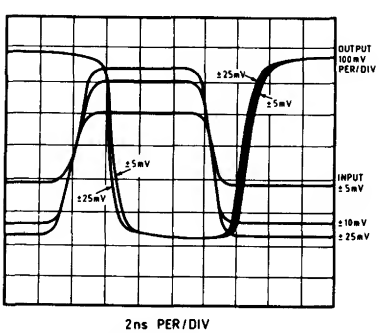


Fig. 14 Response to various input signal levels.

PLESSEY
Semiconductors

SP9750

HIGH SPEED COMPARATOR

The SP9750 is a high speed comparator with a latch circuit and other facilities intended for use in the construction of fast A–D converter systems. The speed capability of the device is compatible with conversion rates of up to 100 Mega-samples per second. Input and output logic levels are ECL compatible.

FEATURES

- Latch Set-up Time 2ns Max.
- Max. Input Offset Voltage 5mV
- Propagation Delay 3ns (Typ.)
- ECL Compatible
- Comparator Output Gating
- Wired OR Decoding for 4 Bits
- Current Output Settling to 0.2% in 8ns

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	–5.5V
Reference supply voltage	–8.5V
Reference current output	15 mA
Input voltage	±4V
Differential input voltage	±6V
Power dissipation	500 mW
Operating temperature range	–30°C to +85°C
Storage temperature range	–65°C to +150°C
Lead temperature (soldering 30 sec)	300°C

Logic input voltages to gate and latch V_{EE} to 0

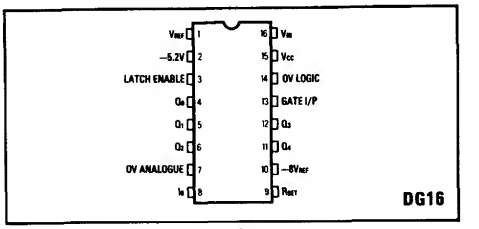


Fig. 1 Pin connections

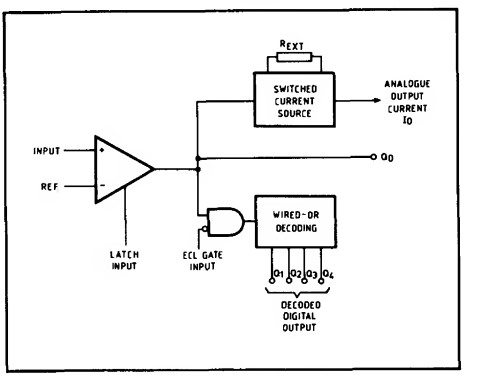
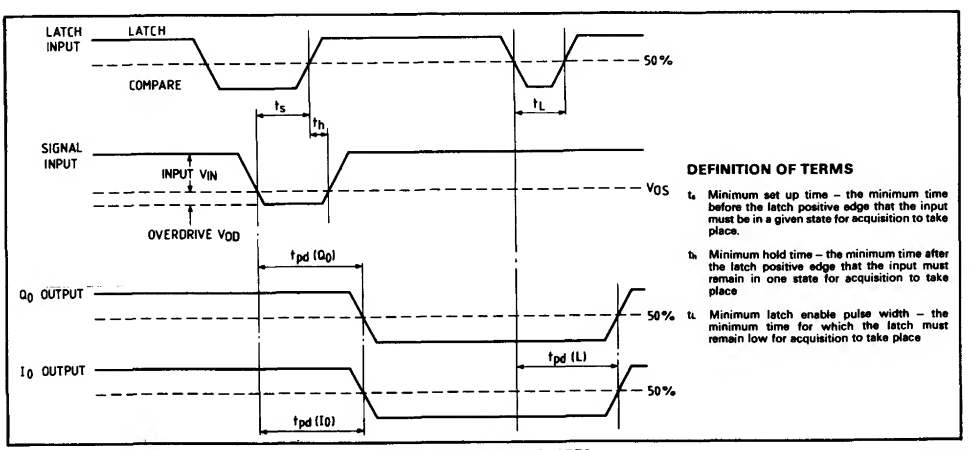


Fig. 2 Block diagram of SP9750



DEFINITION OF TERMS

t_s Minimum set up time – the minimum time before the latch positive edge that the input must be in a given state for acquisition to take place.

t_h Minimum hold time – the minimum time after the latch positive edge that the input must remain in one state for acquisition to take place

t_L Minimum latch enable pulse width – the minimum time for which the latch must remain low for acquisition to take place

Fig. 3 Timing diagram SP9750

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = +25°C
V_{CC} = +5V ±0.25V
V_{EE} = –5.2V ±0.25V
V_{REF} = –8V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	–5		+5	mV	
Input bias current			25	µA	
Input offset current			5	µA	
Supply currents Vcc		16	20	mA	
V_{EE}		35	42	mA	
V_{REF}		14	18	mA	
Total power dissipation		390	470	mW	
Analogue O/P current 'on'		5		mA	See operating note 1
Analogue O/P current 'off'			5	µA	+5V on pin 8
Precision current stability		20		ppm/°C	Also depends on R_{EXT}
Min. latch set-up time (t_s)			2	ns	See operating note 2
Input to Q_o O/P delay (tpd (Q_o))		3	4.5	ns	V_{IN} = 100 mV, 25 mV over drive, 50Ω load
Input to I_o delay (tpd (I_o))		3	4.5	ns	on I_o to 0 volts (Note 3)
Delay gate input to Q_{1-4} high		1.5	2.5	ns	See operating note 4
Delay gate input to Q_{1-4} low		1.5	2.5	ns	
Latch to I_o (tpd (LI_o))					
between 50% points		3	4.5	ns	
to 1% settling		4	8	ns	See operating note 5
to 0.2% settling		8	12	ns	
Min. hold time t_h		1		ns	
Min. latch pulse width (t_L)		2		ns	
Common mode range	–2.5V		+2.5V	V	
Diff. mode range			5	V	
Node capacitance I_o		3.5		pf	
Node capacitance analogue input			3	pf	
Input resistance	60			KΩ	
Output logic levels					
Logic '1'	–.98		–0.78	V	Vcc = +5V, V_{EE} = –5.2V
Logic '0'	–1.85		–1.6	V	R_L = 220Ω to –2V

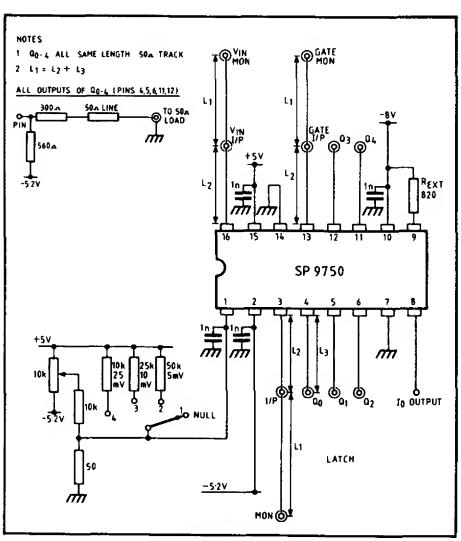


Fig. 4 test circuit

GENERAL DESCRIPTION

The SP9750 is a fast comparator combined with a latch facility which allows the device to be operated in the sample and hold mode.

When the latch is 'low' the comparator is in the 'follow' mode, and when the latch is driven 'high' the output is locked in the existing state. The latch circuitry will therefore always produce a decision on the input state.

The comparator has a relatively low gain in the follow mode, which assists in achieving an extremely fast response. However, due to the positive feedback action of the latch function, the gain approaches infinity during the latch cycle, thereby ensuring high resolution.

In addition to the basic comparator, the following functions are provided on the chip to optimise the performance of high speed parallel-series-parallel A to D converter systems.

1. An ECL compatible gating function for simplified multi-comparator output logic.
2. Four emitter follower outputs from the gate to provide wired OR decoding for four bits.
3. A precision current source, set by an external resistor.
4. A high speed switch for the precision current to provide a fast and convenient reconstruction of the analogue input. Summing the currents in a multi-level

comparator chain provides the D to A conversion directly for the construction of converters of the parallel-series-parallel type.

The philosophy adopted in the SP9750 makes possible the construction of ultra-fast, high accuracy parallel-series-parallel converters by integrating a significant portion of the system function on the same chip as the comparator. The result is not only to reduce considerably the total hardware count but to reduce the propagation delays where they are most critical, and eliminate redundant operations.

OPERATING NOTES

1. The analogue output current (Io) is set by means of an external setting resistor (REXT) and is equal to the reference voltage on Pin 9 (−8V nominal), divided by 2 x REXT. The accuracy of this reference voltage must be consistent with the conversion accuracy required. The output (Pin 8) compliance is −0.8V to +5.0 volts for correct operation.

2. This parameter is defined with +100 mV input and −10 mV overdrive, corrected to take account of the comparator offset, i.e. the switching threshold effectively is at OV on the input waveform. The relationship between setup time and overdrive is shown in Fig.7. The test circuit diagram, Fig. 4 indicates a method of performing this test.

3. Due to the relatively low gain of the comparator in the unlatched state, propagation measurements are defined with a 25 mV overdrive. The relationship between overdrive and delay is shown in Figs.5 and 6.

4. The gate input accepts an ECL drive. The outputs Q_1 to Q_4 are active when the gate input is at an ECL 'low' level, (−1.75V) and are switched by the internal circuitry. A 'high' gate input (− 0.9 V) switches the outputs to 'low', allowing the bussing of multiple devices onto the $Q_1 - Q_4$ rails.

5. Output settling times are measured at 10 mV overdrive conditions; larger overdrives produce shorter delays.

6. The test arrangement shown in Fig. 4 provides for a simple dynamic test of the SP9750 functions. When the switch is in position 1, the input offset voltage is nulled with the potentiometer, a condition detected by observing the output to be at the mid-point of its range (I_o or Q_o). The latch must be 'low' for this measurement. The offset voltage can be measured with a high impedance instrument. Positions 2, 3 and 4 provide increasing amounts of bias to the reference input corresponding to overdrives of 5mV, 10 mV, and 25 mV. For convenience of operation, the input analogue signal is referred to ground, and the reference input is set above ground, so that an input waveform which is positive going and referred to ground is all that is necessary. It should have an amplitude of (100 mV + overdrive voltage) and should have less than 5% overshoot. The risetime should be about 2 nS. Simple circuit modifications and a negative going signal would provide for inputs of opposite polarity. For accurate timing, the path length L_1 should be equal to $L_2 + L_3$ properly terminated.

Static (DC) measurements can also be performed on the same test arrangement.

Performance curves. Unless otherwise specified, standard conditions for all curves are $T_{AMB} = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.2V$, $V_{REF} = -8.0V$, I_O load = 50Ω

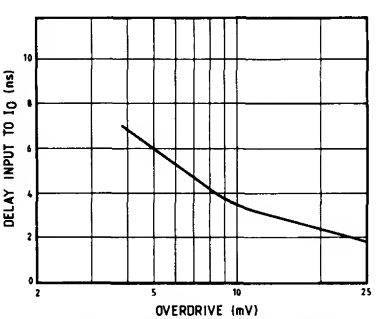


Fig.5 Input to I_o output delay v. overdrive

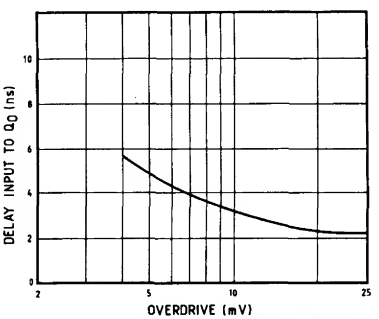


Fig.6 Input to Q_o output delay v. overdrive

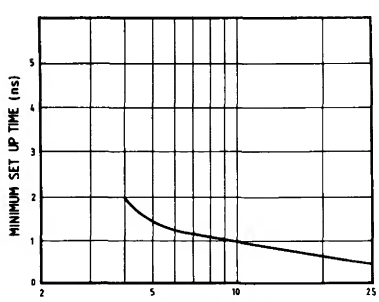


Fig.7 T_s v. overdrive setup time

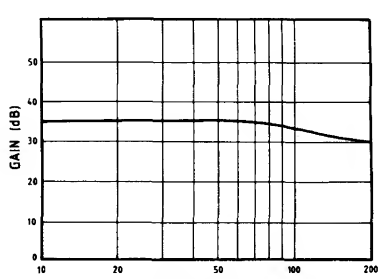


Fig.8 Small signal gain v. frequency (to Q_o output). Latch input low.

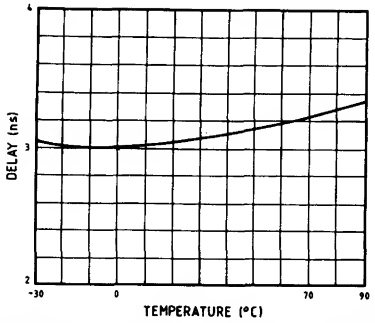


Fig.9 Input to I_o output delay as a function of temperature

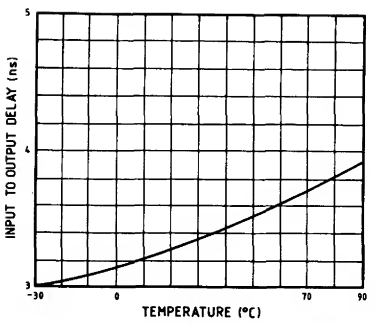


Fig.10 Input to Q_o output delay as a function of temperature

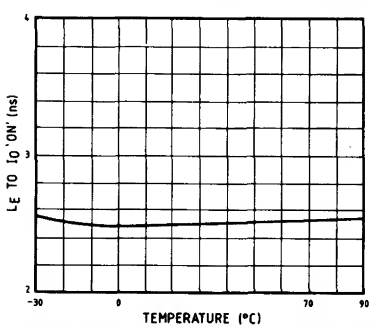


Fig.11 Latch enable to I_o 'on' delay as a function of temperature

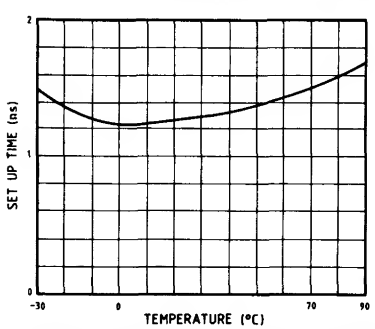


Fig.12 Minimum set-up time as a function of temperature

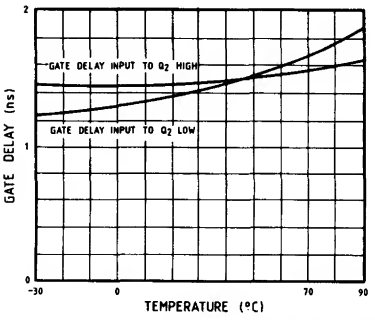


Fig.13 Gate input to $Q_1 - Q_2$ delay variation with temperature

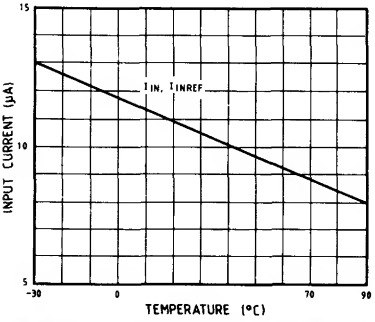


Fig.14 Input current variation with temperature

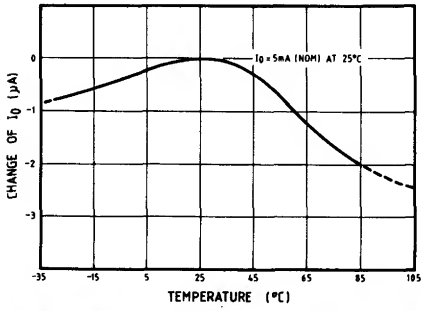


Fig.15 Analogue output current variation with temperature

PLESSEY
Semiconductors

SP9752

TWO BIT EXPANDABLE A TO D CONVERTER

The SP9752 is a circuit block containing four comparators with associated decoding logic intended for use in the construction of A-D converter systems where the ultimate in speed performance is required. Input and output logic levels are ECL compatible.

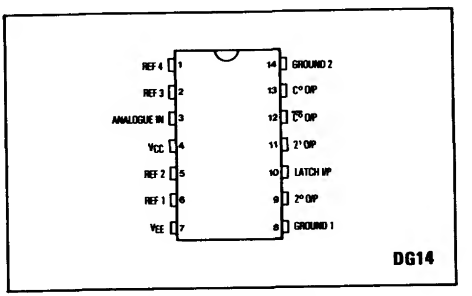


Fig.1 Pin connections

FEATURES

- Minimum Set-Up Time 2nS
- Maximum Input Offset 5mV
- Latch to Output Delay 4nS
- Maximum Clock Frequency 125 MHz
- Four Comparators in 16-Lead Pack
- On-Chip Decoding with Carry and $\overline{\text{Carry}}$

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{AMB} = 20°C
V_{CC} = 5.00V ±0.25V
V_{EE} = -7.00 ±0.25V
R_L = 50Ω (equivalent)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	-5		+5	mV	$R_{SOURCE} < 100\Omega$
Input bias current		14	40	μA	
Reference input current		4	10	μA	
Supply current I_{CC}		41	60	mA	
Supply current I_{ee}		76	90	mA	
Total power dissipation		750		mW	
Min. latch set-up time			2	nS	
Latch to output delay		4		nS	Input o/d > 10mV
Min. hold time		4		nS	
Min. latch pulse width		4		nS	
Max. clock frequency		125		MHz	
Input capacitance		6.2		pF	
Latch input capacitance		2.6		pF	
Common mode range	-2.0		+2.0	V	
Output logic levels					
Output high	-.96		-.81	V	Standard ECL
Output low	-1.85		-1.65	V	
Operating temp. range	-30°		+85°	°C	500 LFPM air flow

GENERAL DESCRIPTION

Following the concept of the SP9750 and SP9685 high speed latched comparators, the SP9752 contains four comparator elements with master-slave latches in a configuration optimised for use in fast parallel, or combination series-parallel A-D converters. Each comparator has a relatively low gain in the track mode, followed by a latch stage conferring essentially infinite gain in the hold mode to produce an unambiguous decision. On-chip decoding logic converts the master latch outputs into binary coded format, then slave latches hold the information through the clock period for maximum system flexibility. The provision of a complementary carry out ($\overline{Co}$) eases the decode logic requirement. It is anticipated that most system designs using the SP9752 will be realised in ECL 10k logic for high speed operation with a minimum package count. Logic inputs to, and outputs from, the device are fully ECL compatible.

The basic comparator circuit is shown in Fig.3. Transistors TR1A, TR1B, TR2A, TR2B provide high input impedance, low offset, modest gain in the track mode, but are switched off in 'hold' when the cross-coupled pair TR5A, TR5B provide the latch function.

The slave latches are essentially simplified versions of the master latches. Master-slave action is determined by on-chip timing operations, and produces essentially glitch-free output conditions which are a pre-requisite of a successful multi-chip converter.

DYNAMIC TESTING

High speed testing of devices of this kind is necessarily a difficult undertaking and the suggested circuit shown in Fig.4 should be carefully constructed if accurate results are to be obtained. The test arrangement is designed to select a single comparator and to measure the response times from the latch to the outputs. Input to output delay are difficult to deal with due to the master/slave action; more relevant are the set-up and hold times.

Operation is as follows:

1. Select the comparator to be tested by S3.
2. Select position 1 on S2.
3. Adjust for a middle state of the outputs using S1. The output should be randomly triggered by noise into alternate states.
4. Set up offset (2mV, 5mV or 10mV) on S2 and measure the appropriate delays.
5. Repeat 1-4 on next comparator.

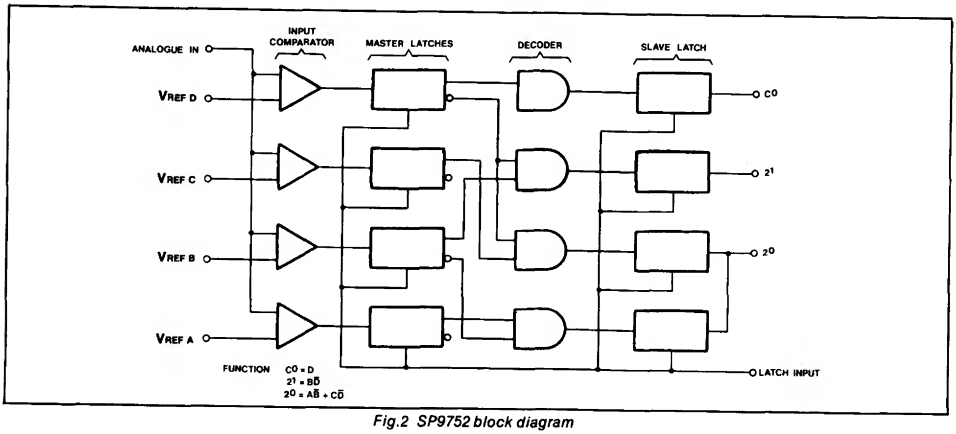


Fig.2 SP9752 block diagram

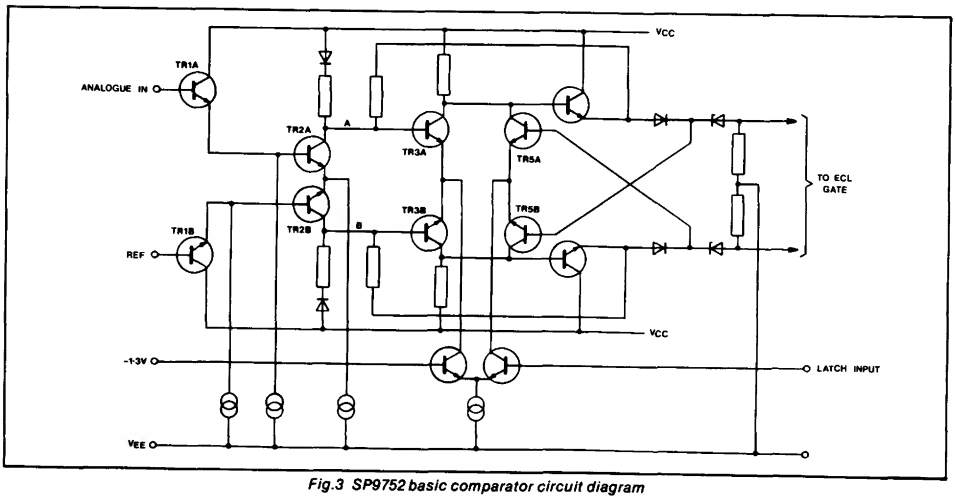


Fig.3 SP9752 basic comparator circuit diagram

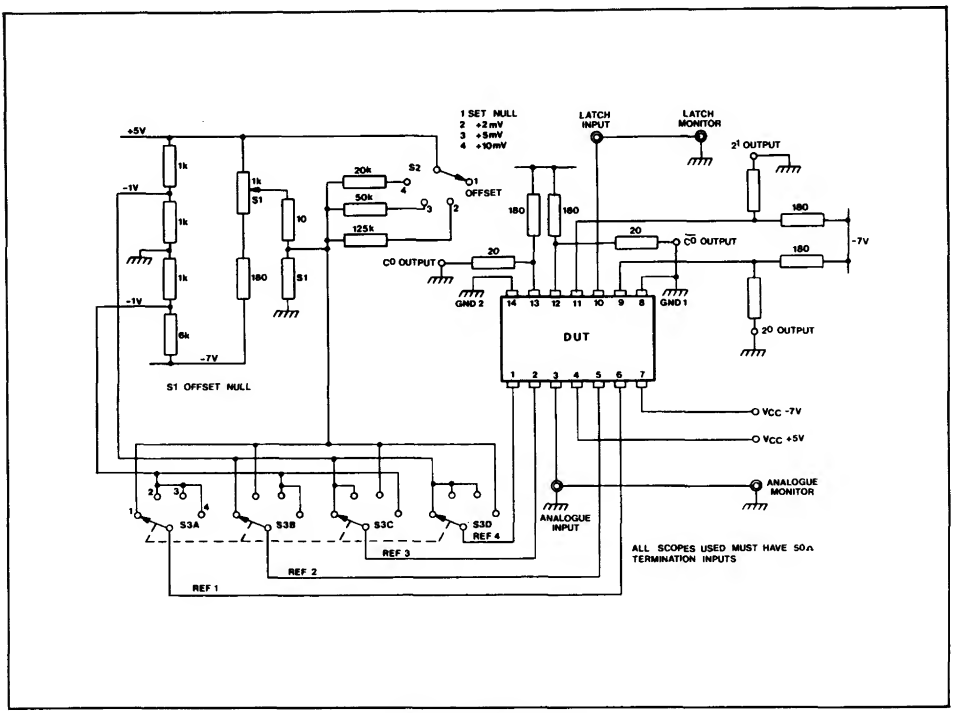


Fig.4 Dynamic test box wiring

APPLICATIONS

5-bit ADC 125 MHz

A five-bit all-parallel ADC is shown in Fig.5. Operation at 125 MHz is possible with no missing codes. Analogue and latch inputs are distributed along transmission lines designed to have matched propagation delays, to minimise latch aperture error. In many applications this avoids the need for a separate sample and hold function. The system input voltage range is ±1.5volts at 50ohms. Encoding is by ECL 10k logic which is the prime speed limitation.

The use of master/slave latching retimes the outputs which are available for the whole clock period.

This converter concept can be extended in principle to nine bits, but practical considerations limit the usefulness in all-parallel systems to six or seven bits, as, for example, seven bits require 32 SP9752s eight bits require 64, etc. In addition, latch and input signal distribution of sufficient accuracy becomes difficult, particularly in relation to aperture error.

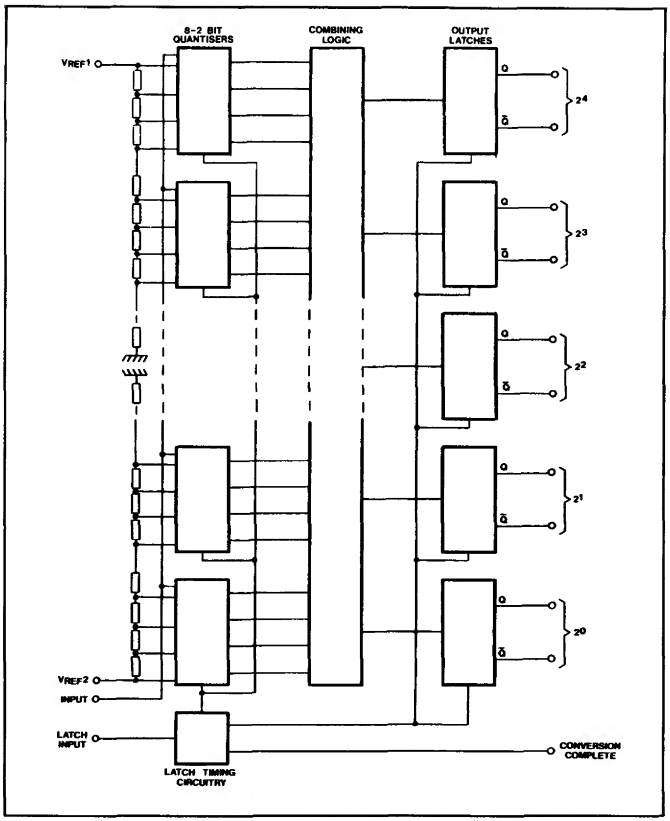


Fig.5 Block diagram of 5-bit A-D converter

PLESSEY
Semiconductors

SP9754

FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A-D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110 MHz, with analogue inputs up to Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous and valid for the complete clock period.

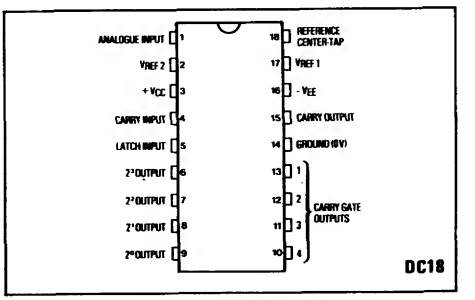


Fig.1 Pin connections

FEATURES

- No External Components For 4-Bit Conversion.
- 110 MHz Conversion Rate.
- On-Chip Encoding For Expansion To 8 Bits.
- No External Sample And Hold Needed.
- On-Chip Resistor Reference Divider.
- Bit Size 10-100 mV.
- ECL Compatible.

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Operating temperature range	-30°C to 85°C
Storage temperature	-55°C to +125°C
Lead temperature (soldering 60s)	300°C

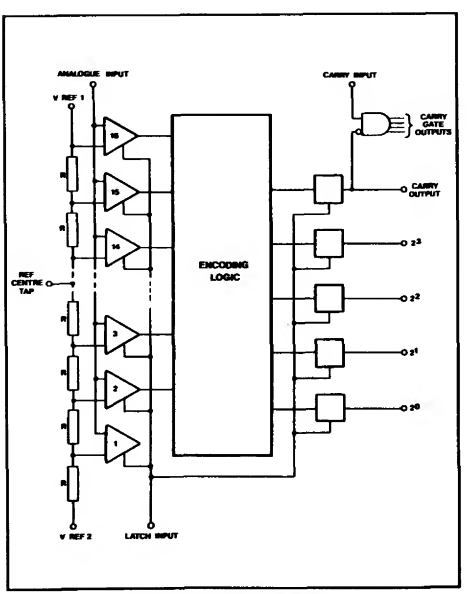


Fig.2 Functional diagram

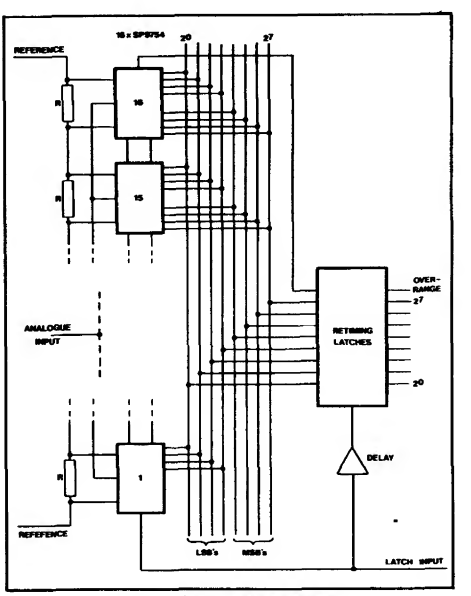


Fig.3 8-bit all-parallel system

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
V_{CC} = +5V
V_{EE} = -7V
R_L = 100ohms to -2V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analogue input current	I_B		30	100	μA	V_{IN} = 0V
Analogue input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	-2		+2	V	
Maximum input slew rate			1000		V/μsec	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I_{CC}		55	70	mA	} See Fig.11
Negative supply current	I_{EE}		85	100	mA	
Reference resistor chain			25		Ω	
Reference bit size		10		100	mV	
Comparator offset voltage	V_{os}	-5		+5	mV	
Total power dissipation	P_{DISS}		950	1160	mW	All outputs loaded
Output logic levels						
Logic high	V_{OH}	-0.930		-0.720	V	} for 100ohm load
Logic low	V_{OL}	-1.90		-1.620	V	} to -2V
Min. latch set-up time	t_S		1.5	2	nsec	10mV overdrive
Latch to output propagation delay:						
Latch enable to output high	$t_{pd}+(E)$		6	8	nsec	
Latch enable to output low	$t_{pd}-(E)$		5	8	nsec	
Carry input to MSB delay	$t_{pd}(C)$		3	5	nsec	
Max. sample rate	$F_{c\,max.}$	100	110		MHz	

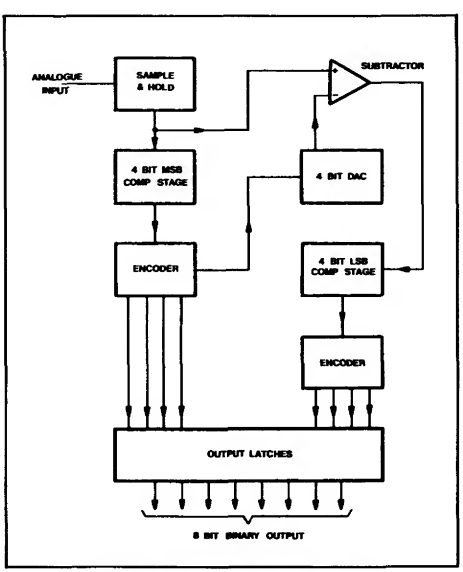


Fig.4 Parallel-series-parallel system

PERFORMANCE CURVES

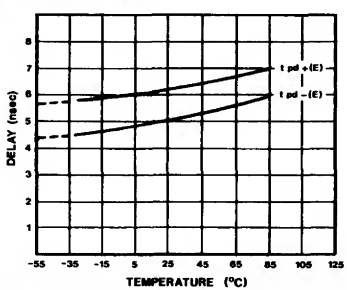


Fig.5 Latch to output propagation delay as a function of temperature

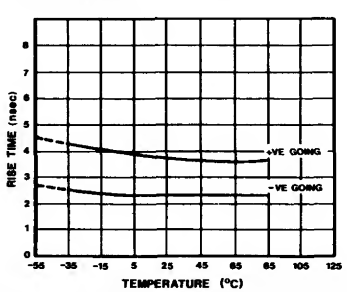


Fig.6 Output rise/fall times as a function of temperature

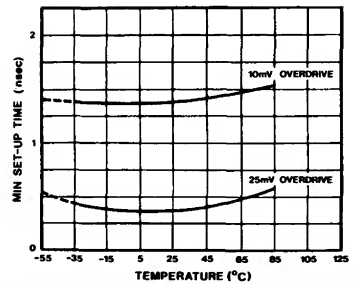


Fig.7 Set-up time as a function of temperature

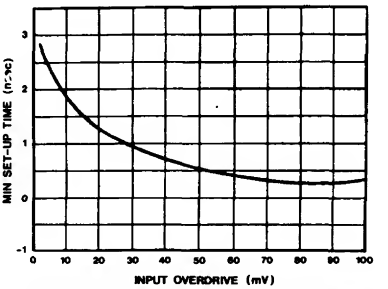


Fig.8 Set-up time as a function of overdrive

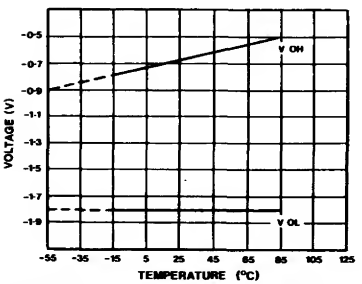


Fig.9 Output logic levels as a function of temperature

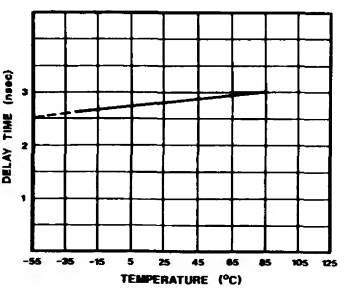


Fig.10 Carry input to MSB output delay as a function of temperature

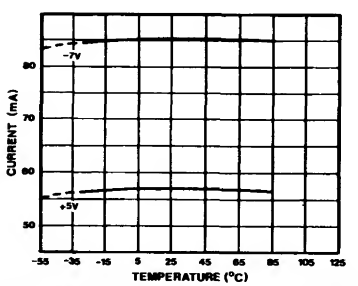


Fig.11 Supply current as a function of temperature

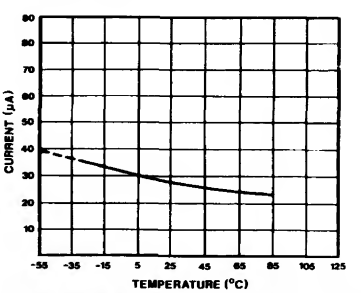


Fig.12 Analogue input current as a function of temperature

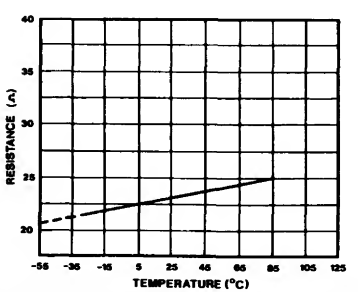


Fig.13 Network resistance as a function of temperature

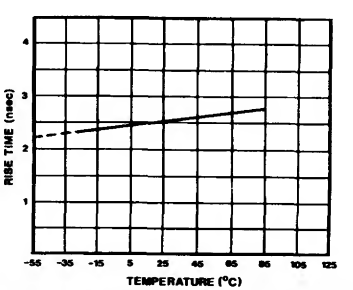


Fig.14 MSB output edge speeds as a function of temperature

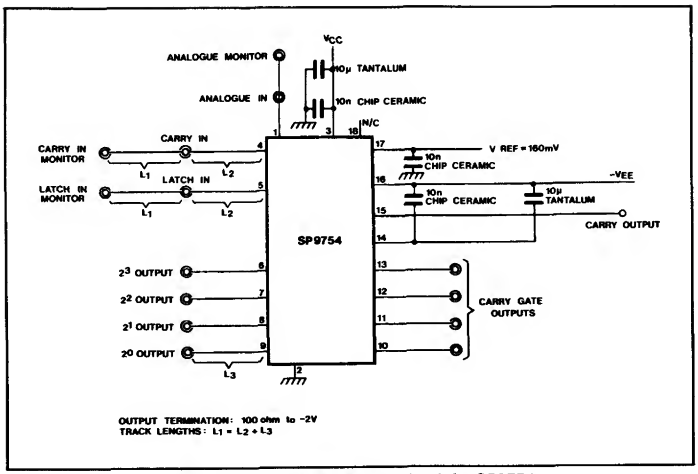


Fig.15 Test and applications circuit for SP9754

PLESSEY
Semiconductors

SP9768

8 BIT DIGITAL TO ANALOGUE CONVERTER

The SP9768 is capable of converting an 8-bit digital signal into an analogue voltage at a rate of over 100 mega-samples per second. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. Included on the chip are a precision voltage reference and a reference amplifier.

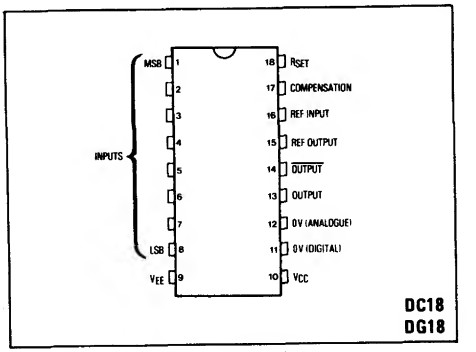


Fig.1 Pin connections

FEATURES

- 5ns Settling Time to ½LSB
- ECL Inputs, Current Output
- Voltage Reference Temp. Coeff. 20ppm/°C
- 100 MSPS Update Rate

APPLICATIONS

- Data Conversion
- Instrumentation
- Video Speed Successive Approximation ADCs

QUICK REFERENCE DATA

Supply voltages: +5V, -5.2V
Power consumption: 400mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage: -6V, +6V
Storage temperature: -55°C to +125°C

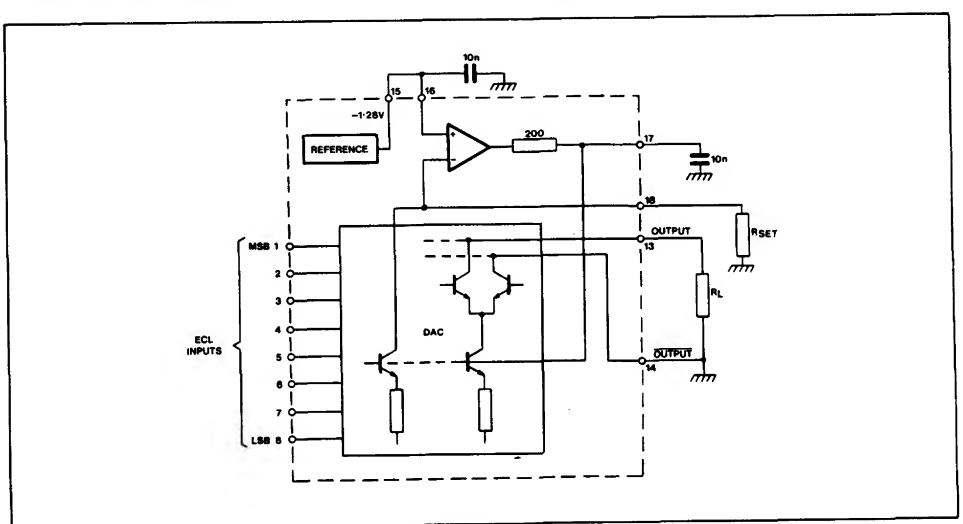


Fig.2 SP9768 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
V_{CC} +5.00V ±5%
V_{EE} -5.20V ±5%
R_L = 50Ω
R_{set} = 220Ω
Input voltage High -0.96V (min) -0.81V (max)
Low -1.85V (min) -1.65V (max)

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Differential non-linearity			0.2	%	
Absolute non-linearity			0.2	%	
Settling time		5		ns	See Operating Note 1
Nominal bit size		78		μA	R_L = 50Ω, R_{set} = 220Ω
		4		mV	
Positive output compliance		+3		V	
Negative output compliance	-1			V	25°C
	-0.7			V	+85°C see Operating Note 2
Multiplying bandwidth		40		MHz	Current mode, see Operating Note 3
Maximum full scale output		30		mA	
Minimum full scale output		2		mA	
Reference voltage		-1.28		V	
Temp coeff of reference voltage		20		ppm/°C	
Zero output		60		μA	
Output current symmetry		100		μA	
Supply current (I_{CC})		12	20	mA	
(I_{EE})		66	80	mA	

CIRCUIT DESCRIPTION

The DAC has current outputs, with a nominal full scale of 20mA, corresponding to a 1volt drop across a 50ohm load, or ±1volt across 100ohms returned to +1 volt. See Operating Note 2.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \quad \text{at full scale}$$

A complementary $\overline{I_{OUT}}$ is also provided. The setting resistor, R_{SET}, is typically 220ohms, and should have a temperature coefficient similar to that of the output load resistor.

Where the load is an oscilloscope, with a 50ohm nominal input, a good quality metal oxide resistor should be used for R_{SET}. It is important to realise that reflections present in 50ohm load systems will often prove to be a limiting factor in the measurement of settling time.

The reference voltage source is nominally 1.280volts and is of a modified bandgap type, average temperature coefficient of 20ppm/°C over the range -55°C to +125°C, corresponding to approximately 1LSB change over this temperature range.

To reduce the possibility of instability or noise generation, the reference supply (pin 15) can be decoupled using a high quality ceramic chip capacitor. Stabilisation of the loop amplifier is by a single capacitor from pin 17 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

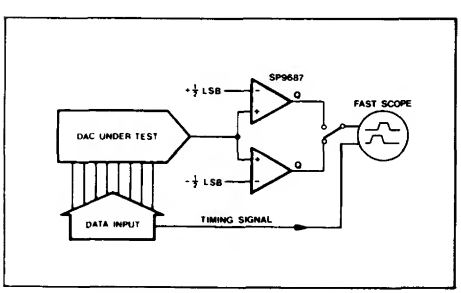


Fig.3 Test schematic (settling time)

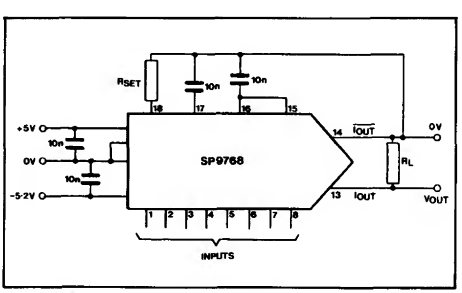


Fig.4 Conventional DAC. Negative output wrt ground.

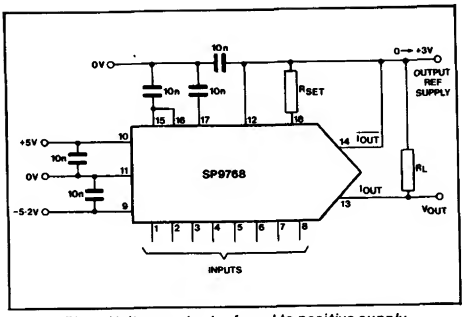


Fig.5 Voltage output referred to positive supply

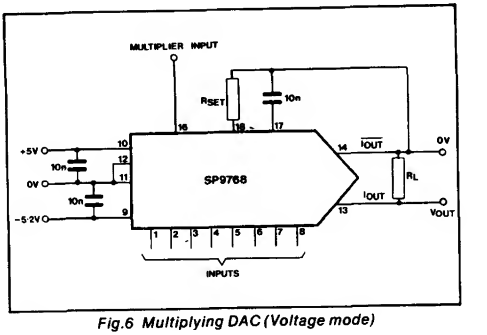


Fig.6 Multiplying DAC (Voltage mode)

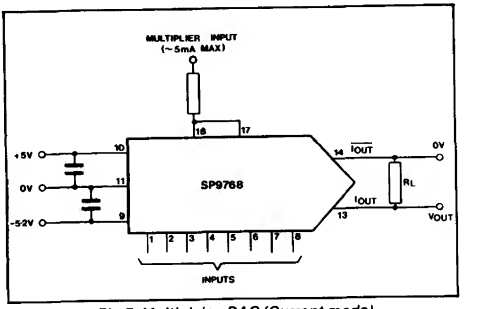


Fig.7 Multiplying DAC (Current mode)

OPERATING NOTES

1. Measurement of Settling Time

The settling time of the SP9768 is measured for a worst case transition of 0 to full scale.

Oscilloscopes, whether real time or sampling, do not have sufficiently low input VSWR or on-screen resolution for precise settling time measurements. A measurement technique has been designed, shown diagrammatically in Fig.3, in which the DAC can settle into a nearly ideal 50ohm load, with minimal interconnection paths; this is also very closely related to the practical use of the device. Precision settling time measurements can be performed with a high speed comparator, conveniently a dual device, such as the SP9687, with a minimal delay time, in this case about 2ns. Two references are set up to detect the DAC output settling within a window, conveniently defined as the settling to ground of the output.

The lower comparator detects the DAC output coming within ½LSB of the final settling point, while the upper device checks that there is less than ½LSB of over shoot.

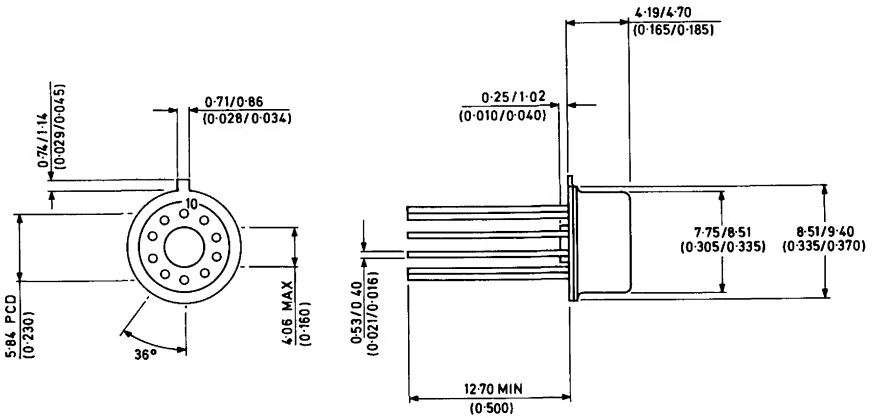
2. Output Compliance

Fig.5 shows the method of using the SP9768 with a load resistor not referred to ground. This connection will be used most often when a larger output voltage than that permitted by the -0.7volt negative output voltage compliance specification is required. The output resistor can be referred to a positive supply in this case as long as R_{set} and the analogue ground are also referred to this voltage. If I_{OUT} is also connected to this reference the decoupling will be simplified.

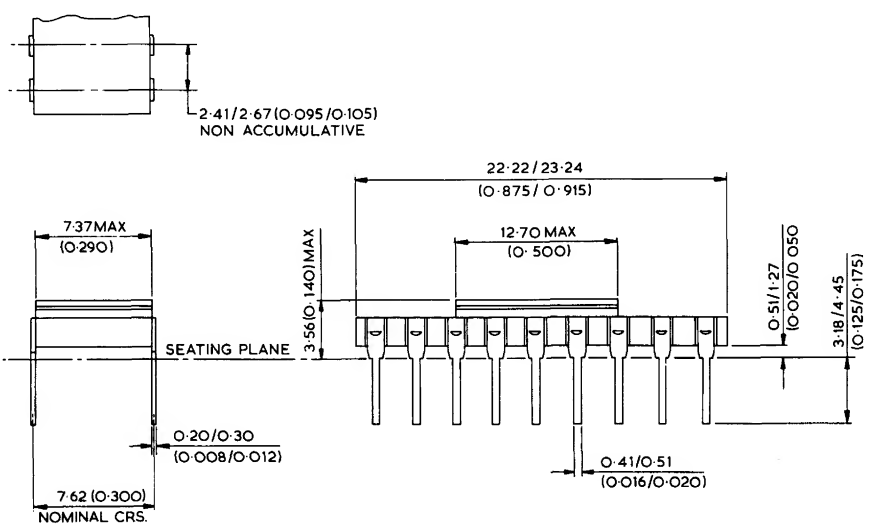
3. Multiplication Modes

Multiplying operation of the DAC is available in two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3dB bandwidth is 250kHz, while in the latter, operational use exceeds 40MHz. Suggested circuits are shown in Figs. 6 and 7.

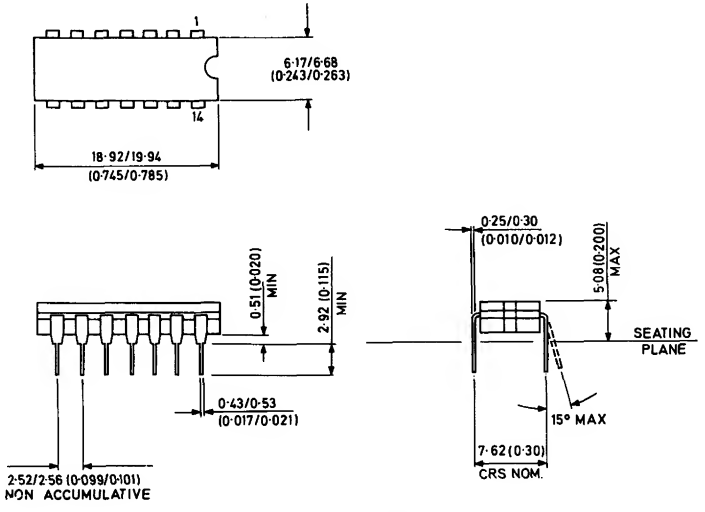
Package Outlines



10 LEAD TO-100 (5.84 mm PCD) WITH STANDOFF **CM10/S**

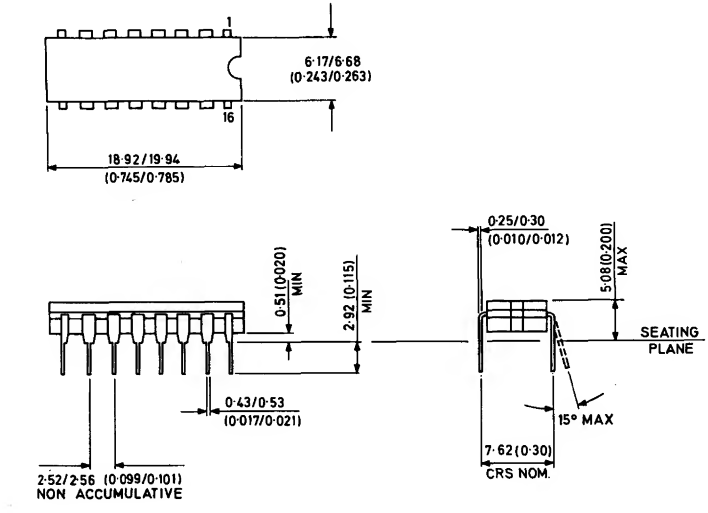


18 LEAD DILMON **DC18**



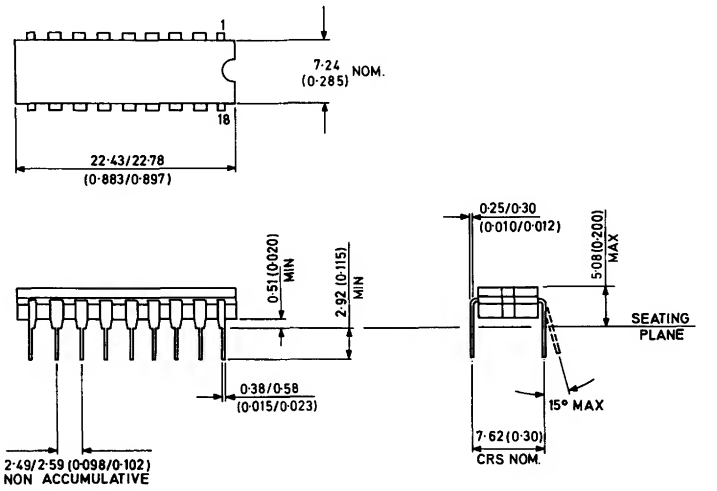
14 LEAD CERAMIC DIL

DG14



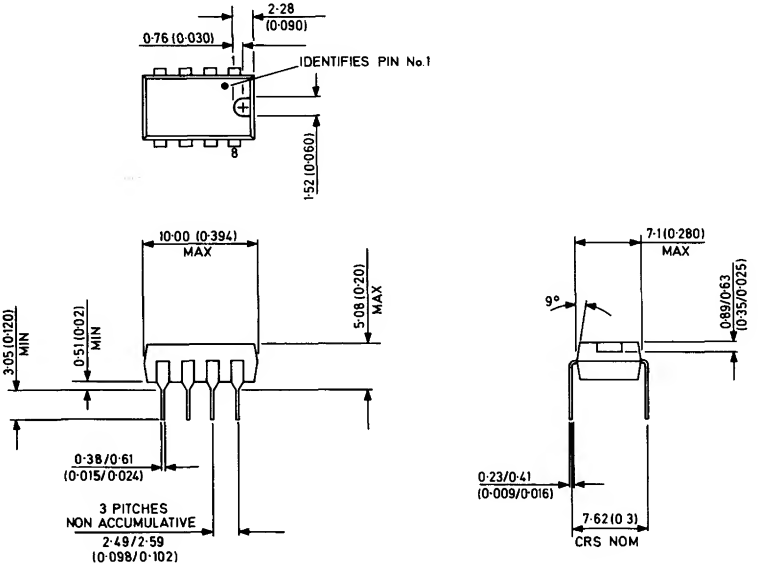
16 LEAD CERAMIC DIL

DG16



18 LEAD CERAMIC DIL

DG18



8 LEAD PLASTIC DIL

DP8

Ordering information

All Plessey Semiconductors integrated circuits are allocated type numbers which must be quoted when ordering.This number may or may not have a suffix(A,B,C,etc.)which denotes the precise electrical specification or temperature grade.When there is a choice of packages the two-digit Pro-Electron code is used to identify the style required,according to the following table:

CM - Multilead TO-5
DC - Ceramic Dual-in-Line(metal lid)
DG - Ceramic Dual-in-Line

Within the UK,orders for quantities up to 99 will be referred to your local Distributor.Quantities of 1000 and over must be ordered from:

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Kembrey Park
Swindon,Wiltshire SN2 6BA
United Kingdom
Telephone : Swindon(0793)694994
Telex : 449637

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